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Surface Insulation Resistance (SIR) Analysis of IPC-B-52 Boards

Purchase Order #: 11111
PAL Report Number: 2000-003

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Date: March 02, 2010

Approved By:

A handwritten signature in black ink that reads 'Joseph M. Rousseau'. The signature is written in a cursive style and is positioned above a horizontal line.

Joseph M. Rousseau
Process Analyst

Objective:

The purpose of this analysis was to evaluate the performance of eight IPC-B-52 test coupons processed with lead-free soldering materials using surface insulation resistance (SIR) testing. The testing was conducted in accordance with IPC-TM-650, method 2.6.3.7.

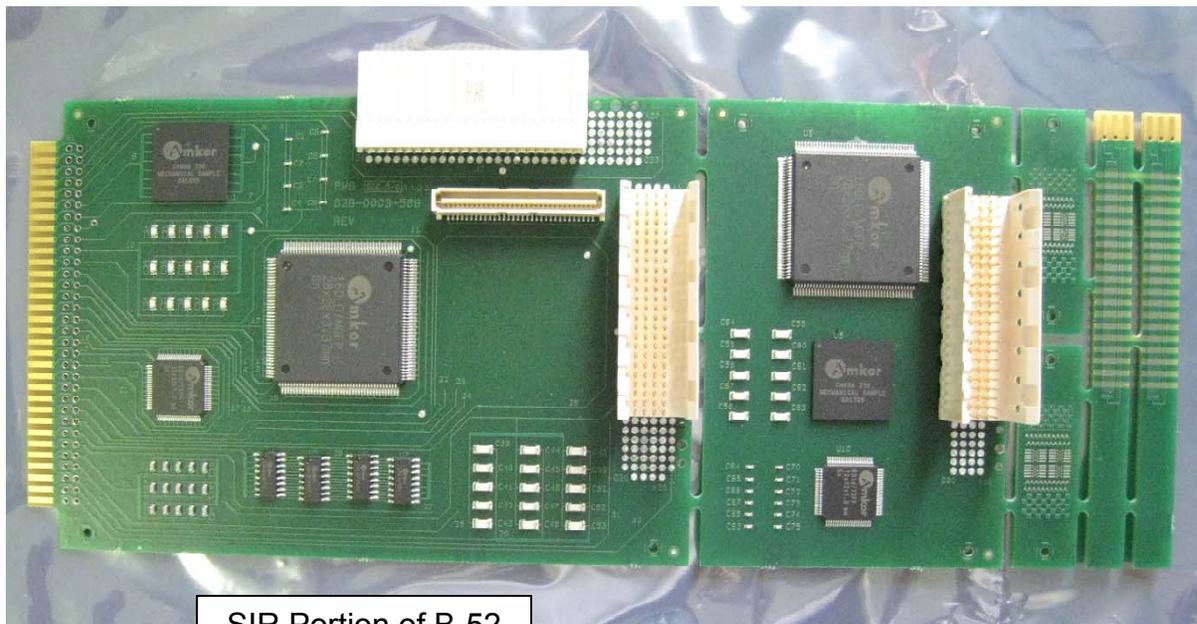
Known Information:

The boards appeared to be made of standard FR-4 epoxy-glass laminate and covered with a green-pigmented solder mask. The surface finish appeared to be a hot air solder leveled (HASL) finish. One board was provided as a “control”. The remaining samples were processed using lead-free solder materials. No other information was provided with respect to the soldering materials or the processing conditions.

Equipment and Materials Used:

- Standard Environmental Systems Test Chamber (calibration due: 12/11)
- Gen3 Systems AutoSIR (calibration due: 10/11)
- Fluke Digital Multimeter (calibration due: 08/11)
- Teflon coated cables

Sample Photograph



Procedure:

1. The interior of the chamber was cleaned with 75% isopropyl alcohol and 25% deionized water (v/v) before any boards were introduced.
2. The deionized water supplying the humidity to the chamber was checked to verify cleanliness before the boards were placed into the chamber environment.
3. All boards were screened for solder bridges and shorts prior to being placed into the chamber using the Fluke multimeter described in the *Equipment and Materials* section of this report. No shorts were identified for this group.
4. The test fixtures were visually inspected for loose and/or broken wires and then checked with a Fluke meter to verify that no wires were broken.
5. The boards were prepared by physically attaching the Teflon coated wires to the appropriate edge-card fingers. The boards were placed inside a clean Kapak pouch prior to any soldering being performed to attach test fixture wires.
6. The AutoSIR was checked prior to testing with a board soldered with precision 100 gigohm resistors.
7. The test samples were suspended in the center of the temperature / humidity chamber using clean Teflon coated wire. The boards were positioned such that the airflow was parallel to the boards.
8. An aluminum rain-shield was installed to help minimize micro-water droplet dispersal from making contact with the boards.
9. An initial measurement (Time 0) set was taken at ambient conditions using a 5 DC measurement voltage and a 60-second electrification time.
10. Upon completion of the initial measurements, the temperature of the chamber was ramped up to 40°C before adding humidity.
11. After a half-hour conditioning period at 40°C, the humidity was then turned on and allowed to slowly ramp up to 90% relative humidity.
12. A bias of 5 DC volts was applied to all boards after the chamber had equilibrated at 40°C / 90% RH for one hour.
13. Measurements were then taken every twenty minutes for the duration of the test.
14. Upon completion of the test, the boards were removed from the chamber and visually inspected.

Results Discussion:

The data for this evaluation is defined in LogOhms. A LogOhm is the base 10 logarithm of the measured resistance: 100 megohms = 1E+08 Ohms = 8.0 LogOhms. Further, the data and charts for this evaluation were too large to include in this report file. As such, they have been attached in a separate Excel file labeled as 2000-003 SIR Data.

Evaluation Criteria

At present, the IPC-B-52 does not have a specified pass / fail criteria defined in any IPC document; however, draft specifications are currently being refined in IPC committees and are expected to be published by late spring of 2011. Doug Pauls, Chairman of the IPC Cleaning and Coating Committees, and the principal designer and researcher of the B-52, is leading this effort. Data has been presented over the past few years on the IPC-B-52 test assembly and the general consensus of the IPC SIR Task Group is that 100 megohms (8 LogOhms) at test conditions is the desired lower level for this test board. As such, the 8.0 LogOhm value was adopted for this evaluation.

There is also a general consensus that data prior to 24 hours of humidity exposure should not be considered towards this criteria. During this time frame, the test vehicle is coming to equilibrium. J-STD-004, the IPC specification on fluxes, has adopted this same 24-hour period before data "counts" in its SIR evaluation of fluxes and flux residues. As the IPC-B-52 test vehicle is largely a vehicle for evaluation of fluxes and flux residues in production, this is a reasonable measure.

In IPC committee meetings, it has generally been agreed that control samples, ones with no exposure of the candidate manufacturing process, should have values above 1000 megohms (9.0 LogOhms) at test conditions after 24 hours. As such, we have applied this value for the evaluation of the control samples.

The final criterion for evaluating an SIR test board relates to the visual inspection of the various patterns and the presence of electrochemical migration (dendritic growth). IPC SIR test methods have varied in the past two decades between 20% and 25% of the intervening space between lines as the maximum dendritic growth allowable without being a failure. Method 2.6.3.7, which represents the most current IPC SIR test methodology, does not specifically give a maximum allowable dendrite. J-STD-004 currently lists 20% as the maximum, which is reasonable for this evaluation.

Analysis Background

For this study, we were asked to evaluate the surface insulation resistance of seven IPC-B-52 coupons processed with candidate lead-free soldering materials. The following is a discussion of the results from those samples and our conclusions (Final Discussion).

Data Discussion

Control Board

We begin the discussion with the unprocessed control board. The control board represents the starting cleanliness condition of the boards prior to any assembly. In reviewing the data for the control, we find that initial resistance levels (taken at ambient lab conditions) were all very good values. Once exposed to the test conditions, the resistance levels dropped several decades. Typically, we would expect a 3 – 4 decade drop during the first few hours of testing, as the boards are still in the process of acclimating to the test environment. Ideally, we would like the resistances remain above 9.0 LogOhms for the duration of the test. Beyond 24-hours, we would expect all of the resistance levels to trend above the pass limit.

For this control board several locations remained below the 9.0 LogOhm limit after the 24-hour grace period. The BGA and SMT Connector sites both recovered to above passing by 36 hours of testing. Other patterns such as the J1, J2 connector sites and both QFP sites and their underlying combs remained below the pass limit for the duration of the test.

Visually, we found no evidence of any water spotting or dendritic growth that might explain some of the low readings. The overall trend of the data suggests that the starting boards were not adequately clean prior to assembly.

Processed Boards

In reviewing the data from each of the processed samples, we find that many of the boards had similar locations with low resistance levels as were noted for the control. The initial readings for several different locations were lower than we would expect. Typically, we would expect the initial readings to be above 10.5 LogOhms or higher.

The J1 and J2 connector sites showed very poor performance for all processed samples for the duration of the test. These same locations were also low for the control. The SMT connector site was below the 8.0 LogOhm limit for all boards, though just barely below for several boards. Again, this was also noted for the control.

The 0805B location, on the bottom side of the board, was below the limit for all boards for the duration of the test. However, the control showed good SIR levels for this location.

All of the surface mount capacitor locations showed good SIR performance despite the presence of heavy flux residue. The 0603 pattern on board 2 had one low reading at 116 hours, which recovered by the following reading. It continued to perform well for the remainder of the test.

The SOIC locations also showed good SIR levels despite heavy flux residues noted for all boards. The BGA location showed good overall SIR performance for all

boards. The BGA site on board 4 was a little unstable compared to the other samples during the early part of the test. It recovered to above the limit by 24-hours and continued to improve for several hours before stabilizing at a very good level.

The results from the visual inspection of the boards can be found in the accompanying Excel file (labeled 2000-003 SIR Data). The visual inspection of the processed cards revealed a number of different items. First, with respect to the J1 and J2 connector sites, heavy concentrations of white and/or brown flux residues were noted on the bottom side of those locations. A few boards had pockets of brown residue on the bottom side of the J1 and J2 sites, which might have been from touch-up operations. Similarly, heavy concentrations of flux residue were noted in the 0805B sites of all boards. Also noted was the adhesive used to attach the chip capacitors to the board prior to reflow.

In addition to the flux residues, we noted several locations with fibers. Fibers can be problematic in that they may absorb sufficient moisture to allow leakage between two opposing conductors.

Other items that were noted were solder balls. Solder balls may be an indicator of several items from improper stencil size to old paste to incorrect reflow conditions. Further, we noted that the SMT connector location was easily damaged during part removal. We observed that the pads lifted very easily and in a few cases the traces also lifted from the board. We have not typically observed these types of issues when we have evaluated this board in the past. Lastly, we noted some discoloration of the solder mask on the bottom side of the control card. In addition, a few boards showed some discoloration of the solder mask over some of the traces.

The following Appendix shows the different visual anomalies that were noted. We did not take photographs of every board, as the items that are shown were common to all of the boards.

Final Discussion

Many of the failed patterns on the processed samples also failed on the unprocessed control sample. The poor performance of the control board suggests that the boards were not adequately clean prior to the start of the test. We suspect that the control board, since it had a HASL finish, contained residual HASL flux. It is common for HASL fluxes to contain halide-bearing (Cl^- , Br^-) activators. If the boards were not adequately cleaned post-HASL, then those residues could lead to low SIR values, which appears to be the case for this evaluation.

Since the starting boards do not appear to be clean, it is difficult to assess the compatibility issues between the solder paste and wave flux. In terms of the solder paste residues, with the exception of the one 0603 reading on board 2, all of the topside surface mount chip capacitor sites showed good SIR levels. All of those locations had considerable flux residue between the pads. Taken together, this data suggests that the solder paste residues alone do not degrade electrical performance.

To contrast, the SMT connector sites were also processed with the same solder paste, but showed poor SIR levels for the entire test for all boards. In addition to noted flux residues, a few boards had fibers that spanned opposing conductors. Some fibers, depending on their composition, can lead to lower SIR levels, but we are suspicious that the boards were not adequately clean in that location. The control board had readings below the 9.0 LogOhm limit for several hours, which eventually recovered and continued to improve throughout the remainder of the test. This further suggests that there may have been residue left from the fabrication processes.

The bottom side 0805B location was processed with not only the solder paste, but also a surface mount adhesive and was exposed to the wave solder flux. The SIR levels for all of the 0805B locations were poor. Again, since the topside surface mount parts were processed with the same solder paste, we don't believe that the solder paste by itself is a problem. The low SIR levels noted for this location may be the result of incompatibilities between the solder paste flux, wave flux and adhesive.

In terms of the J1 and J2 connector sites, the SIR levels were overall very poor for the processed boards. Additionally, both of these sites were low on the control boards as well. Given that the control board showed poor SIR levels in those areas, it is difficult to assess to what extent the low SIR levels are due to the flux or to the starting board cleanliness.

We would recommend working with the board supplier to improve the cleanliness of the boards being shipped to you. We would also recommend re-evaluating this set of materials. However, we would verify the board cleanliness by ion chromatography before spending the time processing the boards.

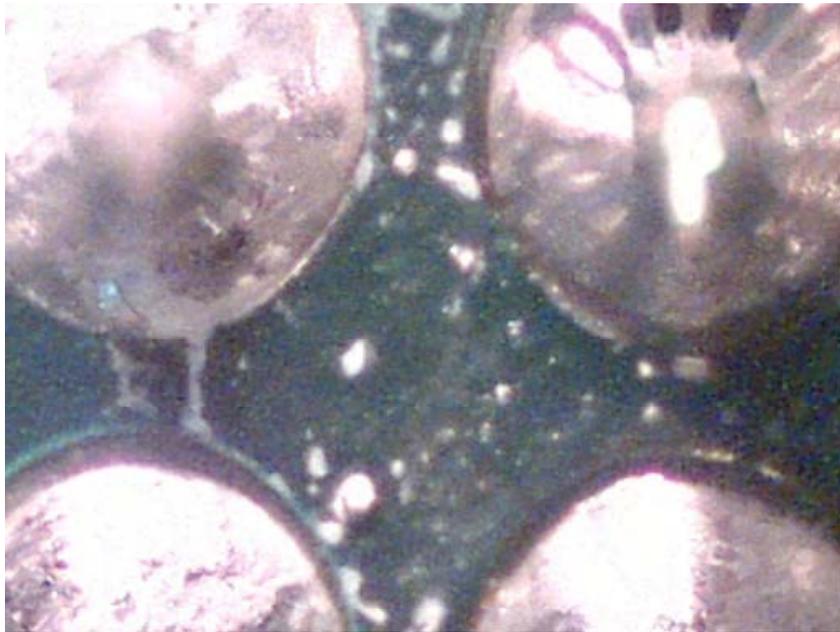
Lastly, the following Appendix contains photographs of the different anomalies noted in this study. Pictures were not taken of every assembly as many of the sites showed similar items.

Appendix – Photographs of Visual Anomalies

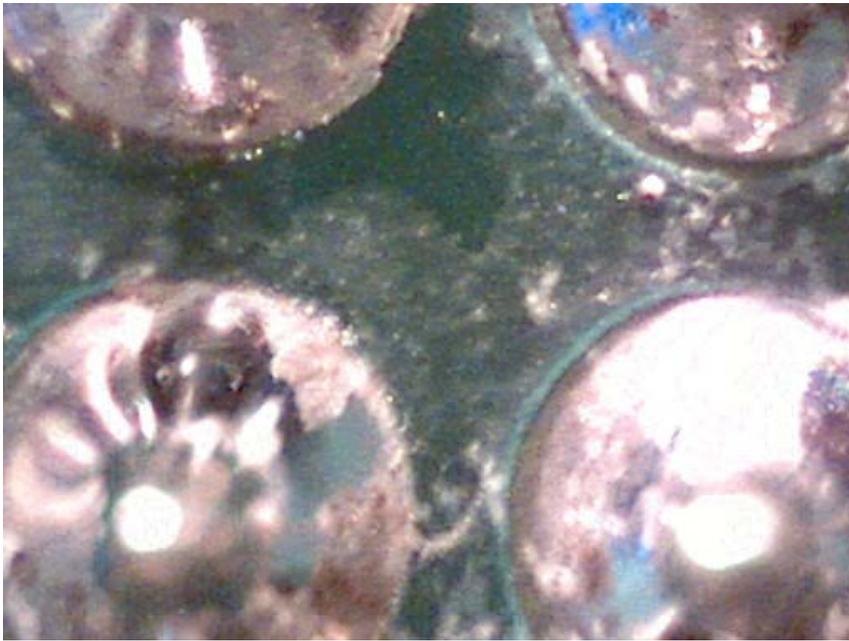
Pattern J1 (flux residue) – Board 1



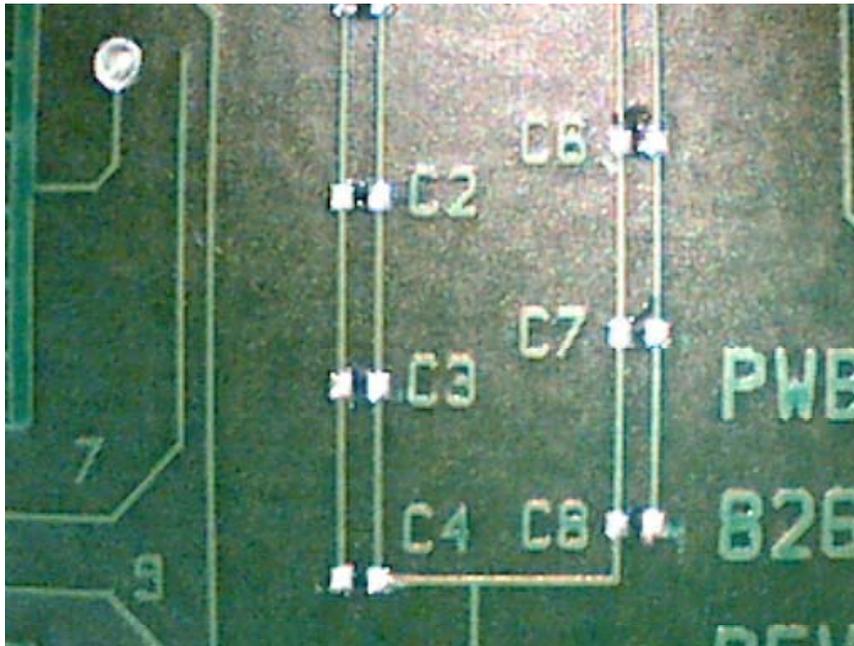
Pattern J1 (flux residue) – Board 1



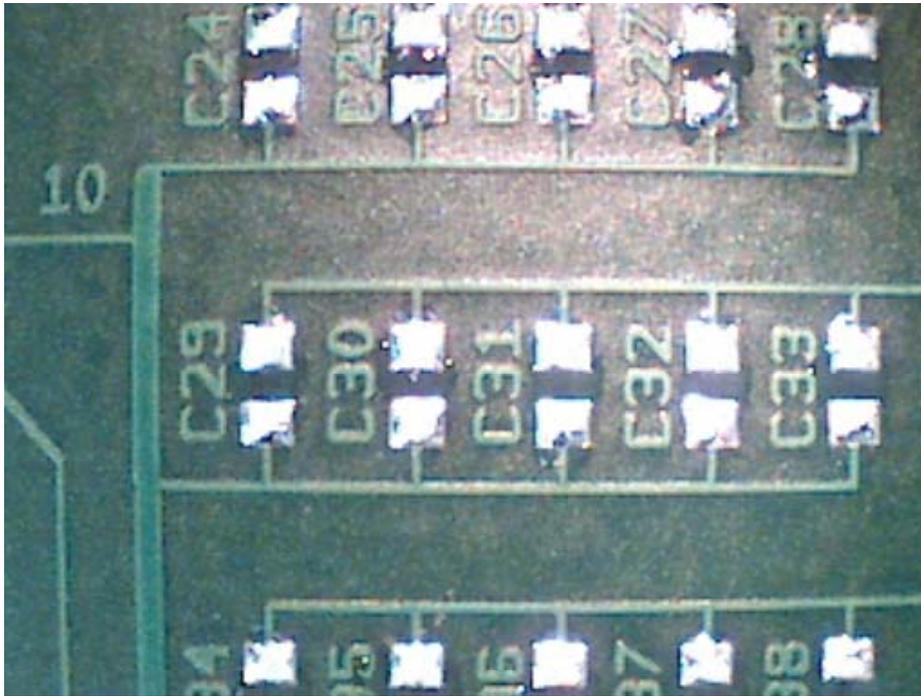
Pattern J2 (flux residue) – Board 1



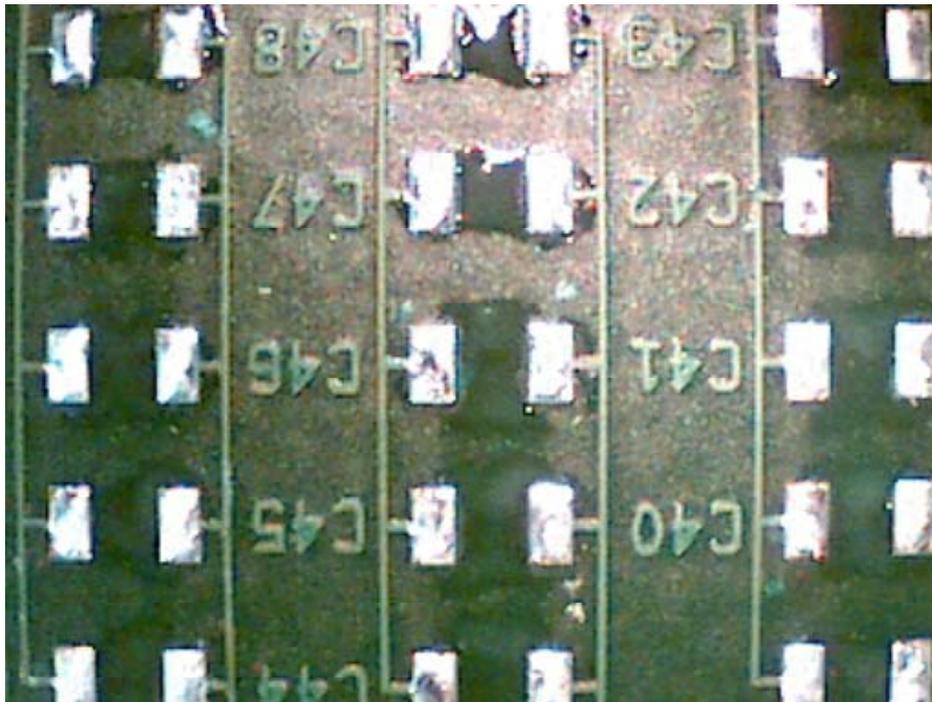
Pattern 0402 (flux residue) – Board 1



Pattern 0805T (flux residue) – Board 1



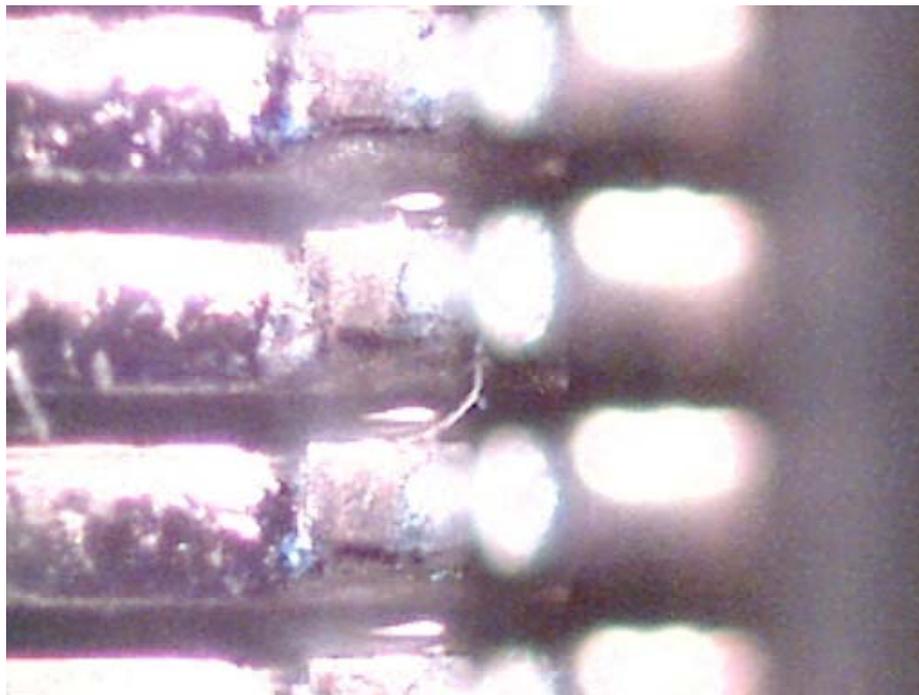
Pattern 1206 (flux residue) – Board 1



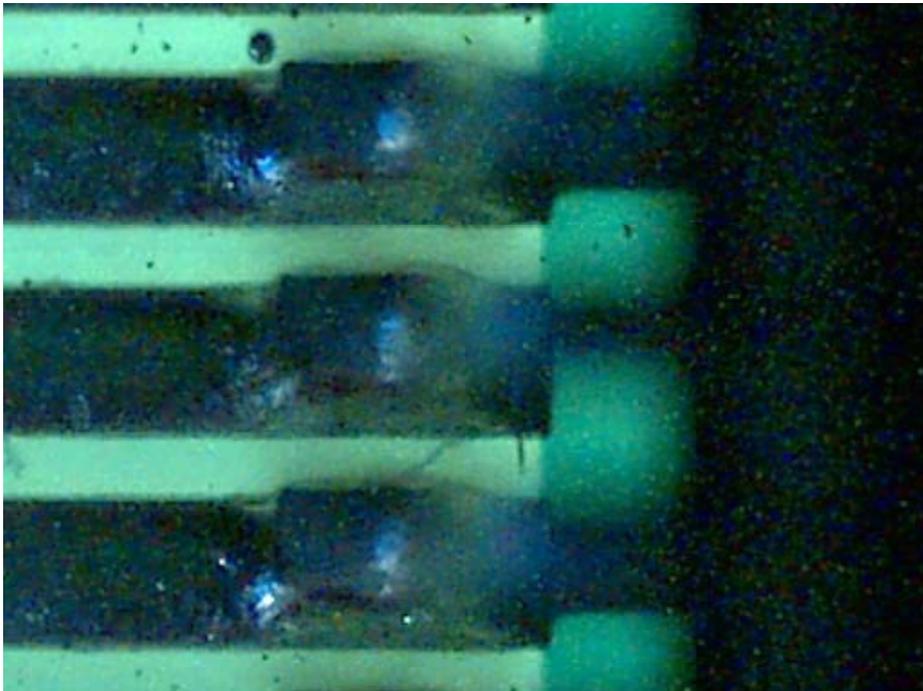
Pattern 0805B (flux residue and SMT adhesive) – Board 1



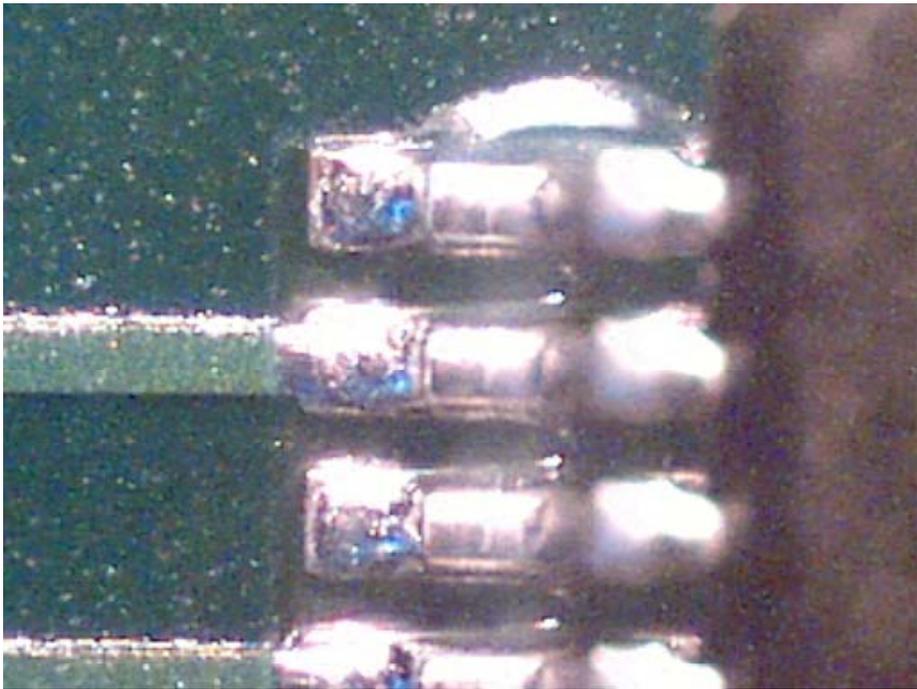
Pattern QFP160 (fiber) – Board 1



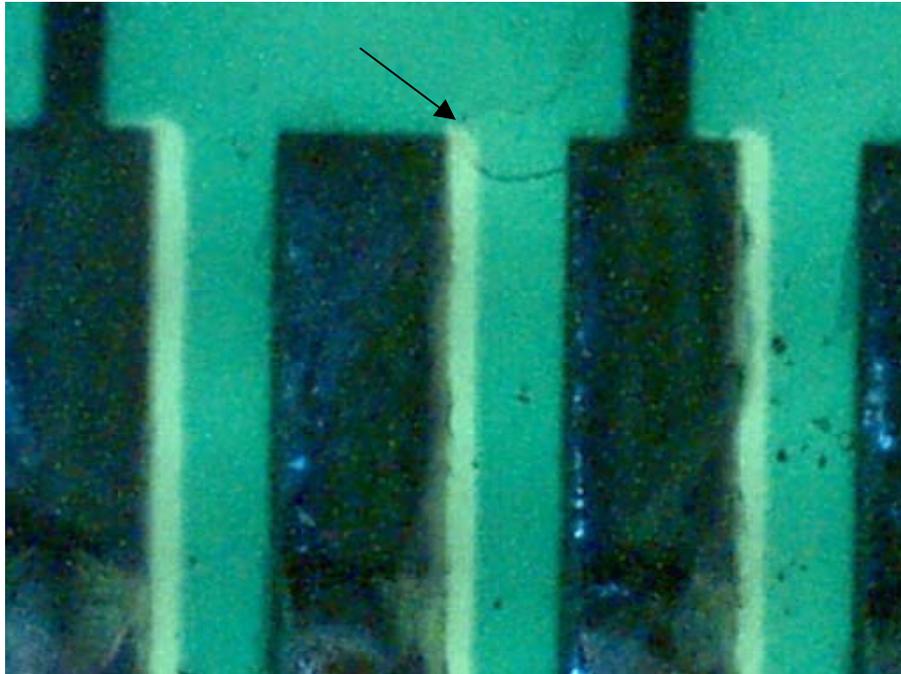
Pattern QFP160 (fiber backlighting) – Board 1



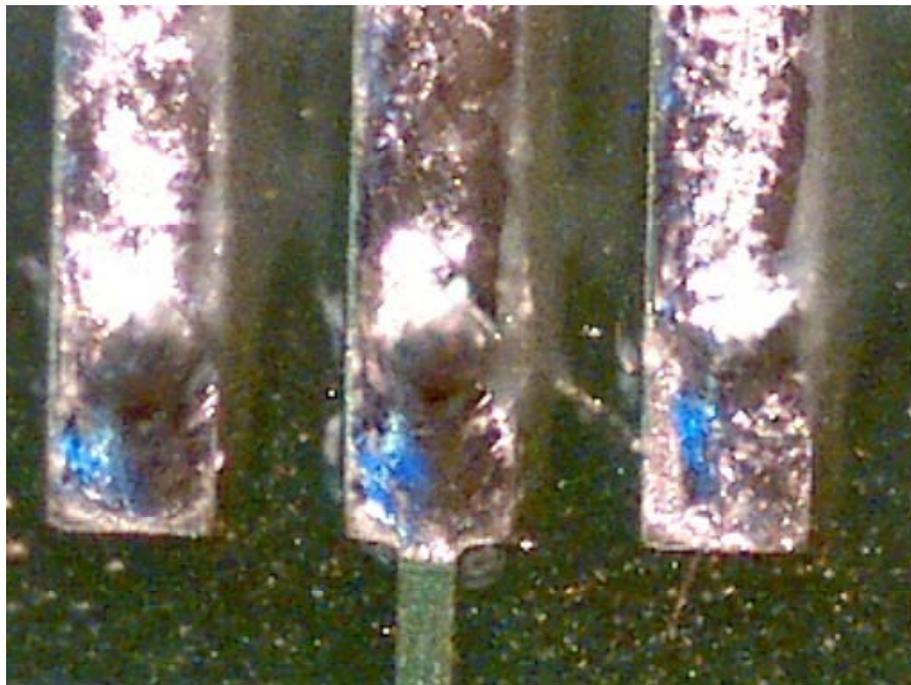
Pattern QFP80 (flux residue) – Board 1



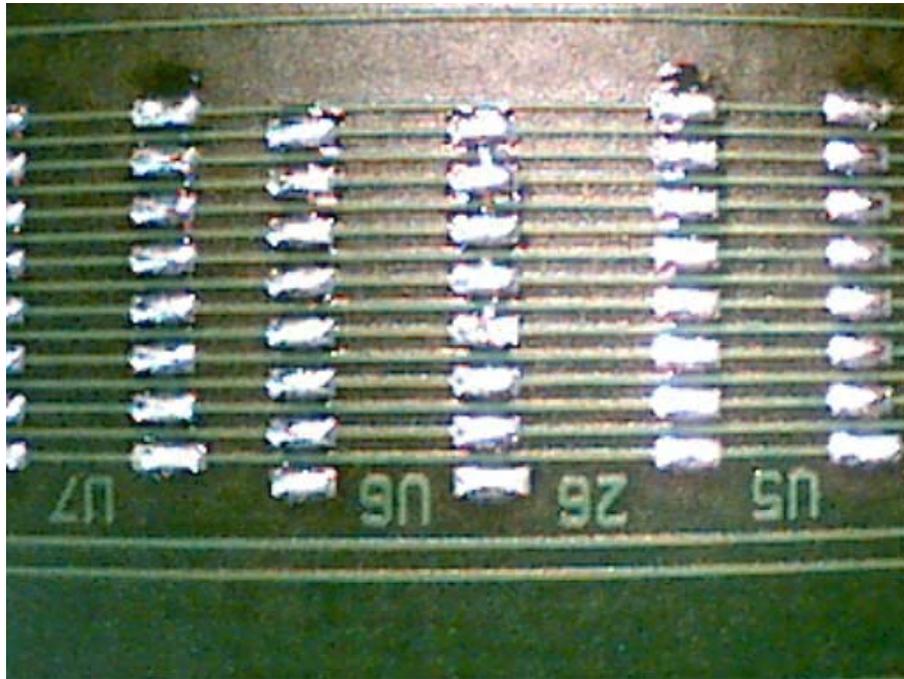
Pattern SMT Connector (fiber backlighting) – Board 1



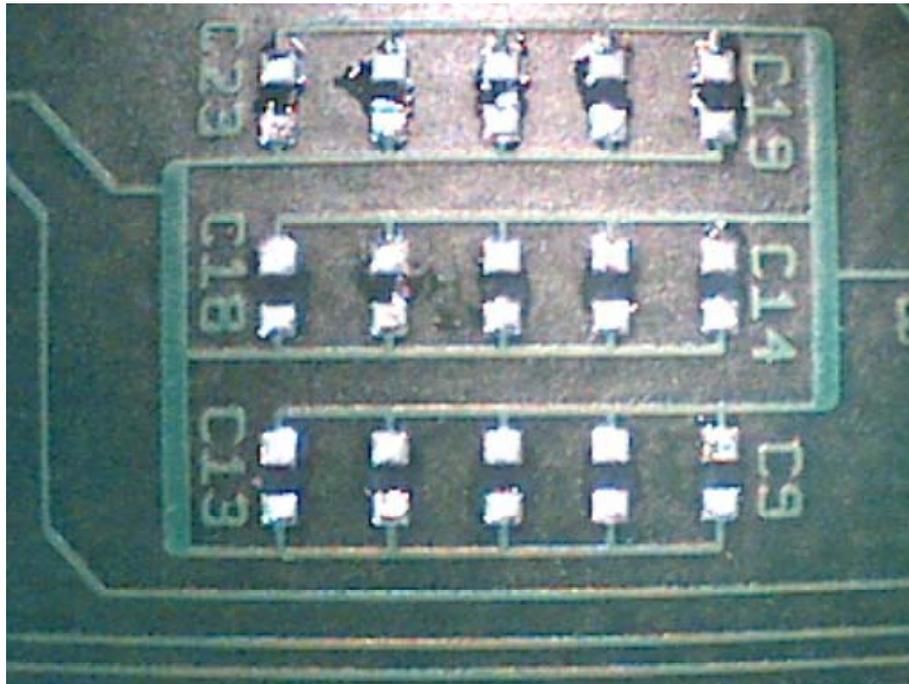
Pattern SMT Connector (fiber and flux residue) – Board 1



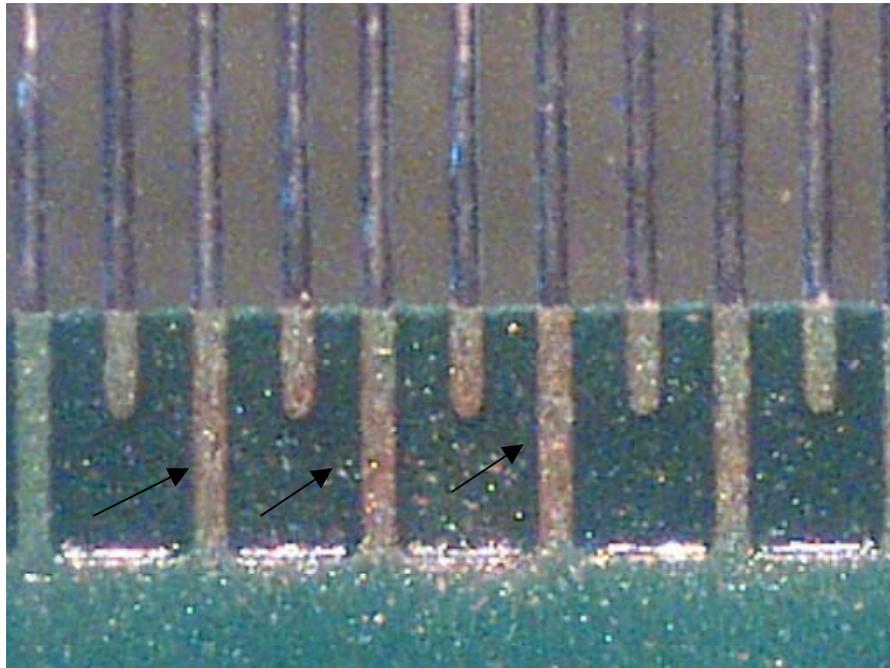
Pattern SOIC (flux residue) – Board 1



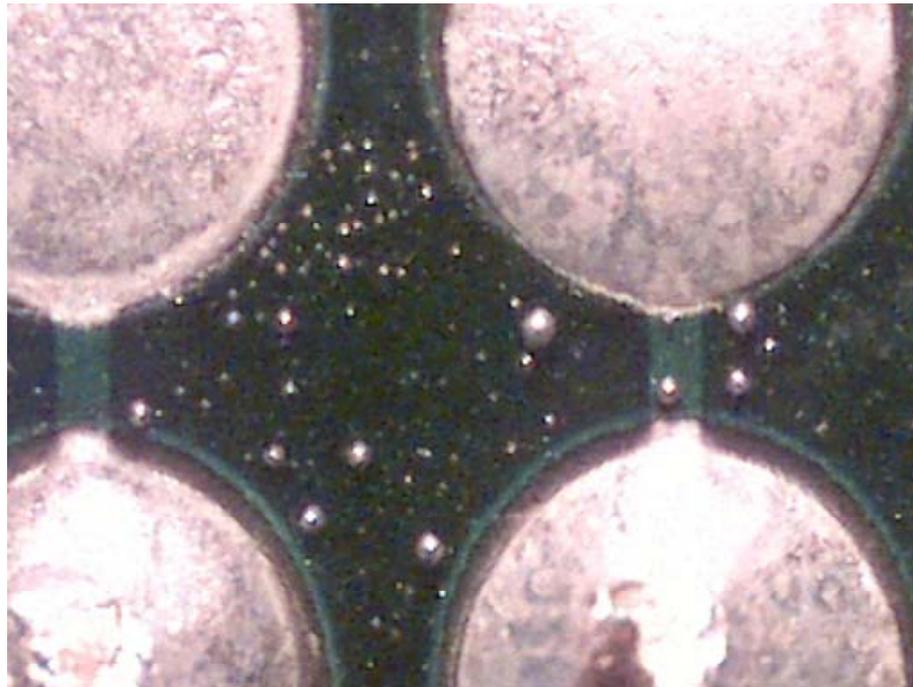
Pattern 0603 (flux residue) – Board 1



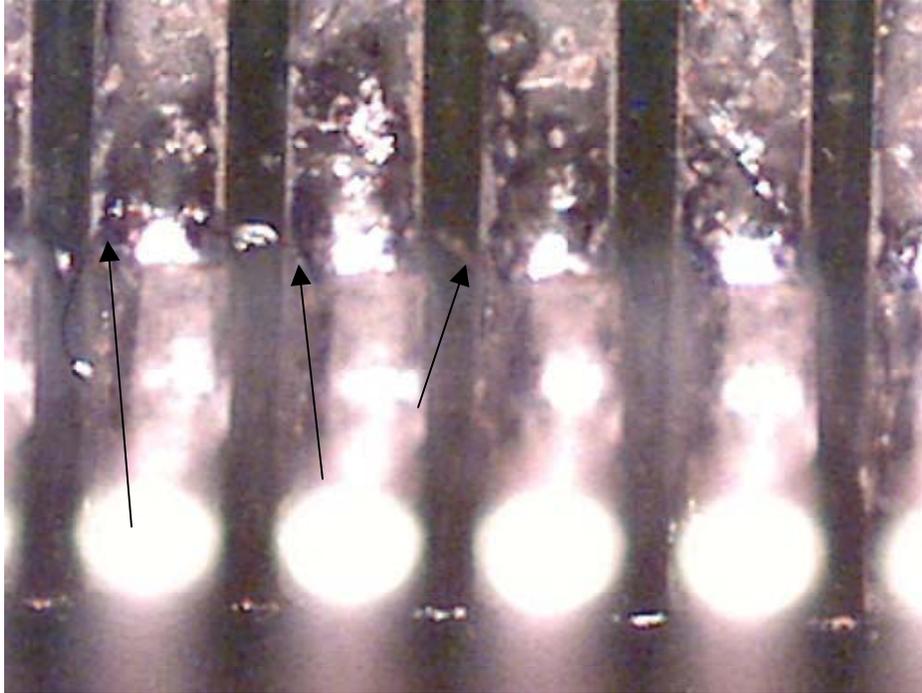
Pattern QFP 80 Comb (solder mask discoloration) – Board 2



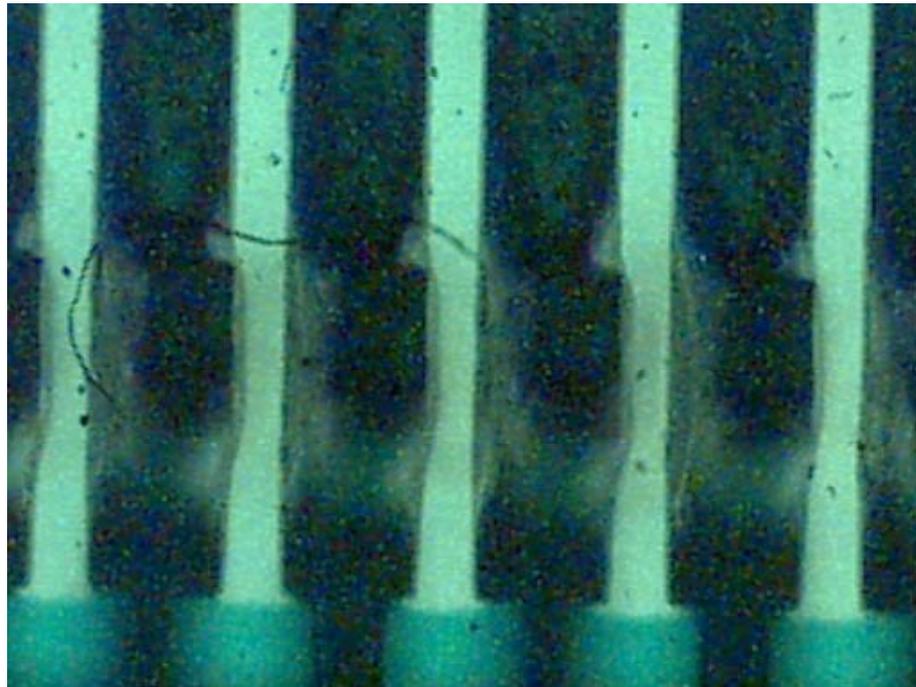
Pattern J1 (solder balls) – Board 2



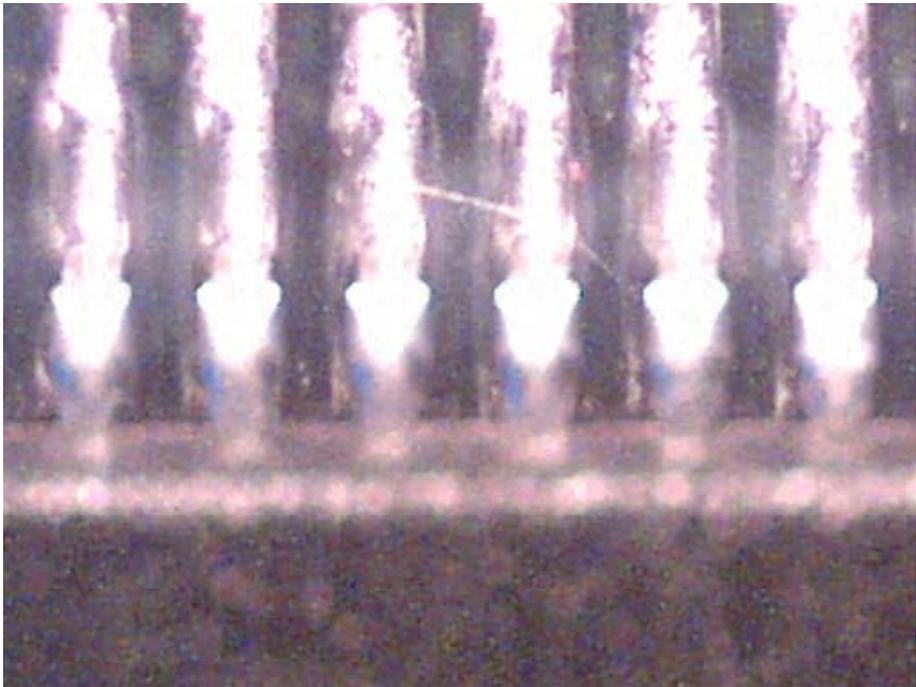
Pattern QFP160 (fiber) – Board 2



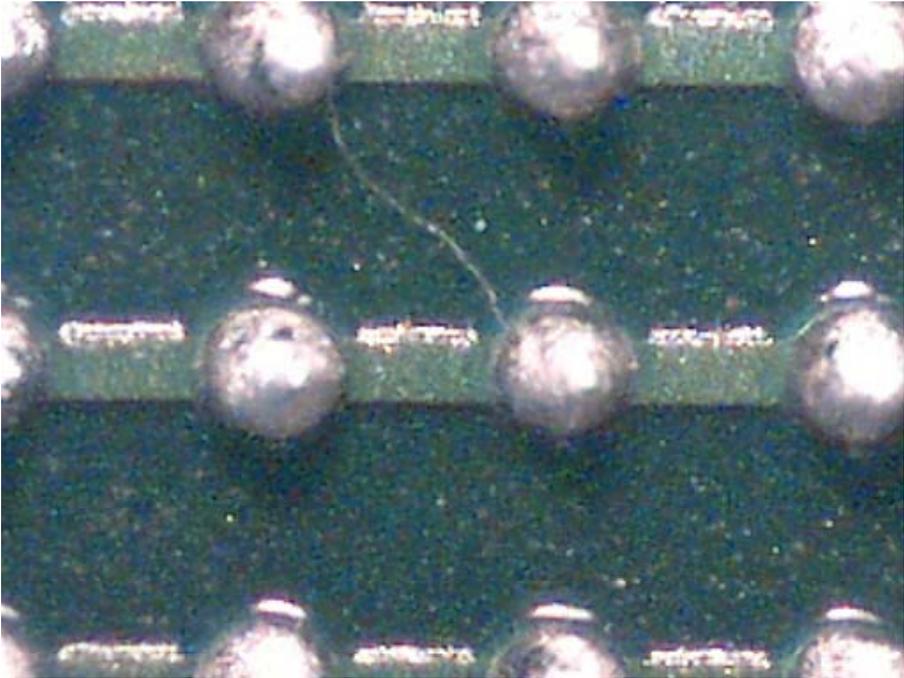
Pattern QFP160 (fiber backlighting) – Board 2



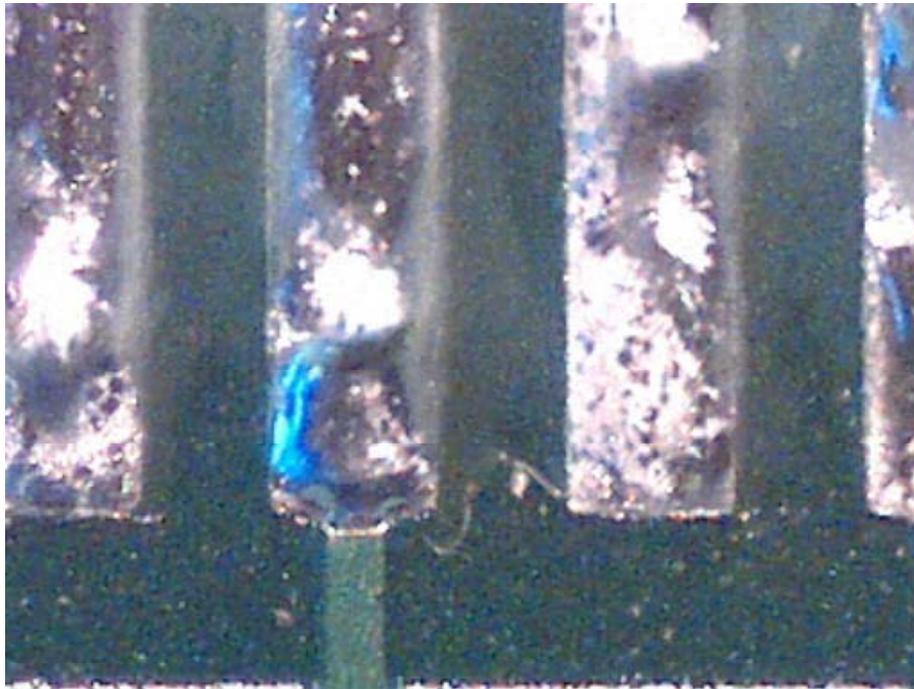
Pattern QFP80 (fiber) – Board 2



Pattern BGA (fiber and flux residue) – Board 3



Pattern SMT Connector (fiber and flux residue) – Board 3



Pattern 0805B (solder mask discoloration over trace) – Board 4



Pattern QFP80 Comb (solder mask discoloration) – Board 4

