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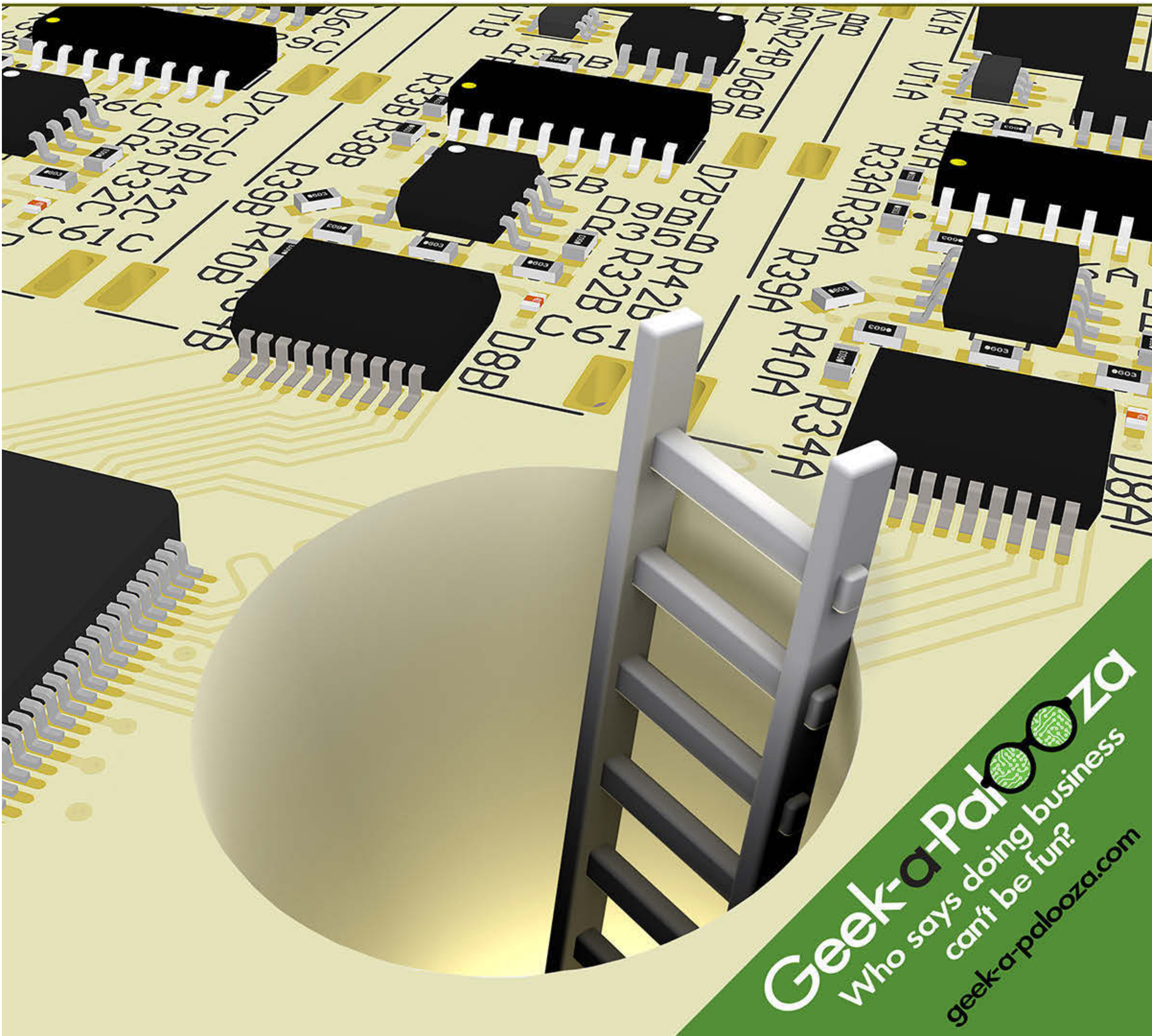
NOVEMBER 2016

THE VIA ISSUE: The Hole Story



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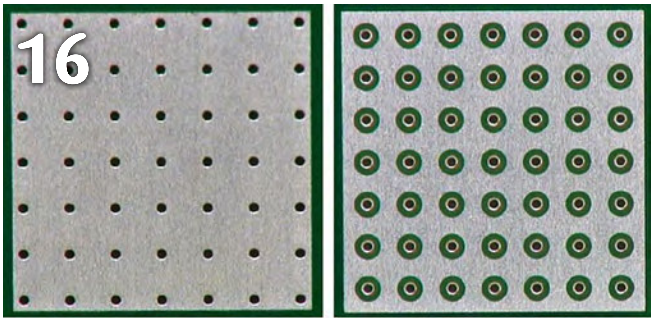

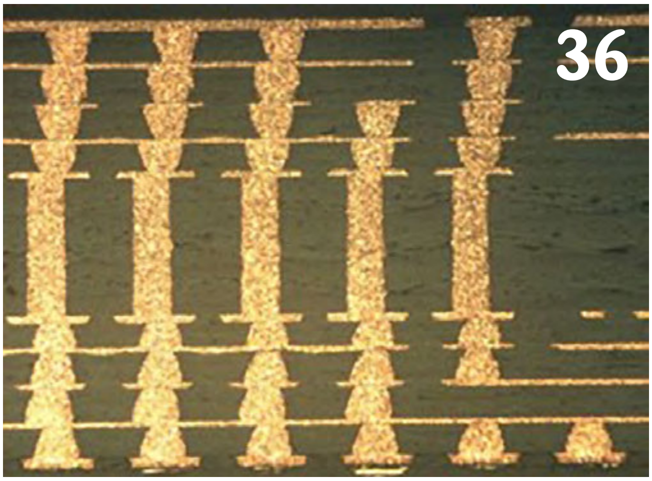

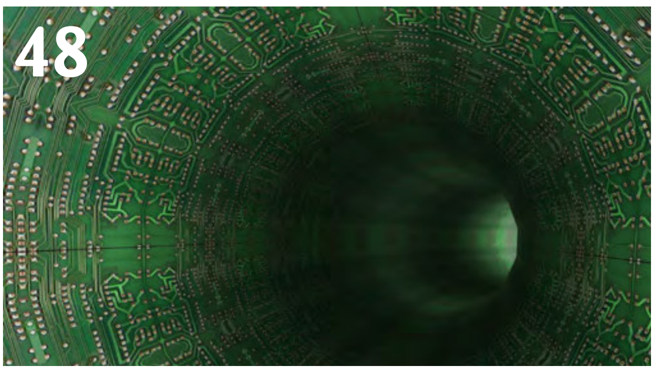

The Via Issue

This issue of *SMT Magazine* looks into the impact of vias on PCB assemblies.

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The Impact of Vias on PCB Assembly

by Stephen Las Marias
I-CONNECT007

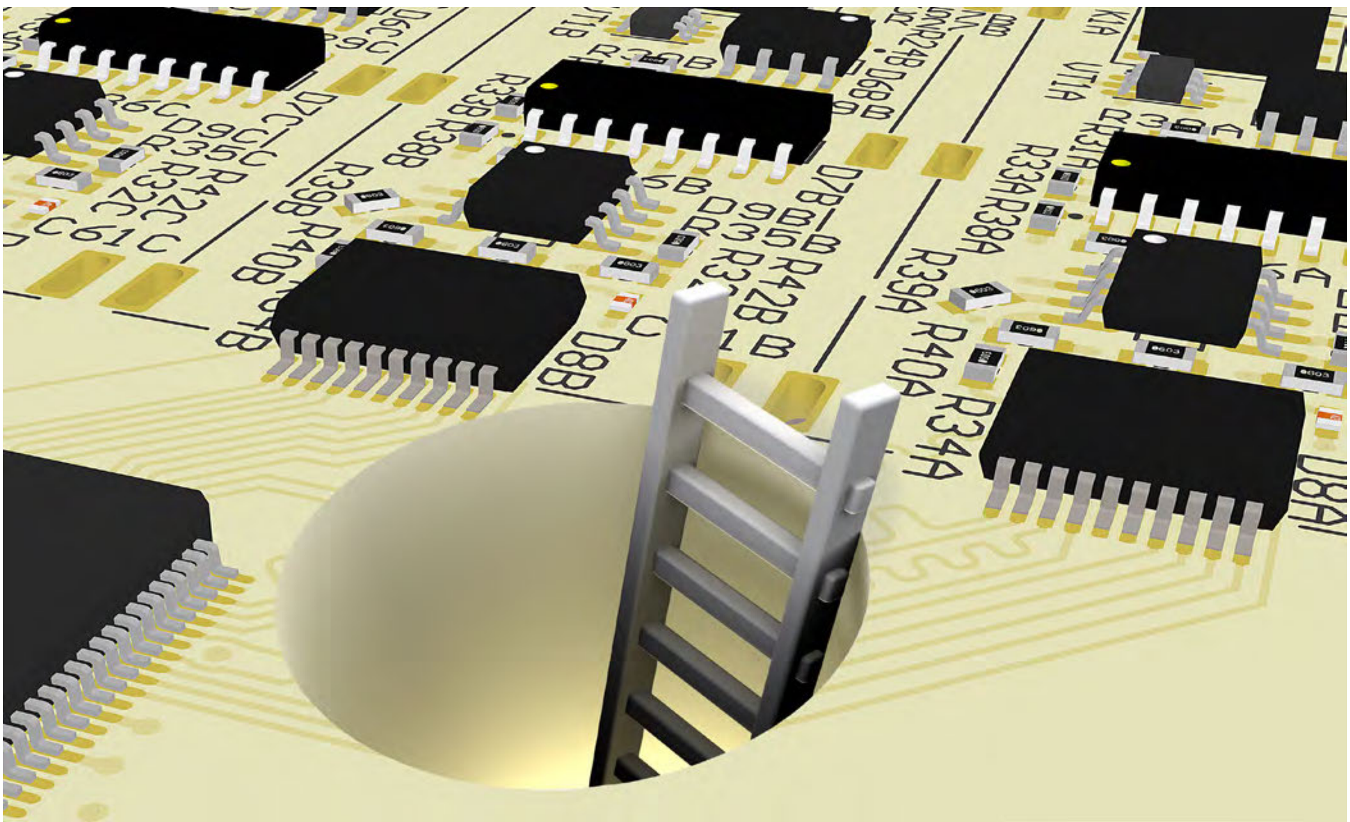
The continuing trend towards smaller and smaller devices with even more functionality has resulted in a dramatic reduction in the size of components, silicon packages, and the PCBs themselves. Component technologies such as BGAs and CSPs have challenged PCB manufacturing technologies due to the number of input/output connections and tighter and tighter pitches associated with these devices. Don't forget the costs associated with fabrication.

Via technology—including blind and buried—has been one of the solutions to address the miniaturization and component density challenges in current electronic assemblies. Advantages include improved electrical and thermal performance; increased wiring density; space-saving in PCBs; placement of even more chips and components in PCBs; and finally, smaller PCBs.

Do You Use Blind Vias and/or Buried Vias?		
Yes		84.44%
No		15.56%

Source: I-Connect007 Survey

However, vias are not without their own set of challenges. In our recent survey that focused on vias, respondents mentioned challenges such as impedance matching, routing, placement of vias, minimum size limitations, aspect ratio, and the limitations for the PCB manufacturer. One respondent commented: "In-pad vias in thermal pads and regular lands often cause processing issues. If they are tented, trapped residues and 'popping' are issues. If they are not tented, solder thieving is an issue. We have also



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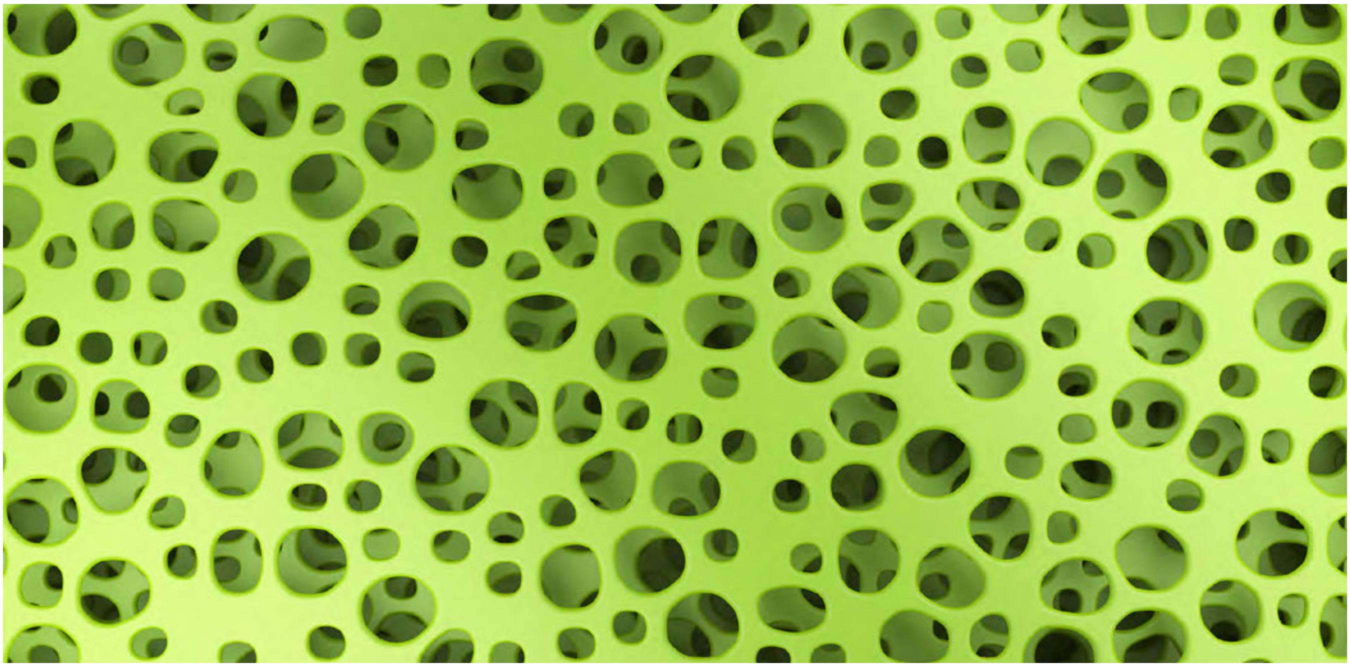


tried using solder mask dams on the pad to prevent thieving with poor results. We also don't want to add more vias than necessary to meet the thermal target. In this case, more is not necessarily better as it may increase voiding at the thermal interface." He added that more vias increase the drill time at the PCB fabricator side, and may increase cost.

Reliability is also an issue, per our survey. One respondent said that their QA department is concerned that tenting vias leaves contaminants in vias, which can affect the long-term reliability of the PCB assembly. He noted, though, that tenting vias help minimize solder problems, so he always tents vias. Apart from tenting, via filling, mask covering and plating are also challenges when dealing with vias.

This brings me to our topic for this month's issue of *SMT Magazine*, which aims to provide more information on the impact of vias in PCB assembly.

For starters, we have W. Scott Fillebrown of Libra Industries writing about why vias are considered the "unsung heroes" of a circuit board. He said vias designed properly complete a circuit, while the opposite can cause reliability nightmares.

Next, David Geiger, Anwar Mohammed and Jennifer Nguyen of Flex discuss a study they conducted regarding the impact of via and pad design on quad flat no-lead (QFN) assembly, specifically on voiding and protrusion. Their study finds out whether a small via prevents the solder to flow to the other side, how the via should be designed, and what via type will have less of a voiding issue.

Patrick McGoff of Mentor Graphics meanwhile looks at the problem of automotive electronics reliability, and improving automotive electronics further by looking at the PCB. He enumerates the critical features of the PCB that you need to measure to assess reliability, including the type, size and number of layers of the PCB, the number and size of vias, microvia stackup, vias in pad, embedded devices, and aspect ratio, to name a few. He also lists the electronic component and padstack details to be used, and finally, the manufacturing process considerations when producing the boards.

In his article, Yash Sutariya of Saturn Electronics/Saturn Flex explains the results of his study on the impact of waiving PCB pre-baking prior to assembly. His study includes via integrity, via life impact, via failure, and overall reliability failures.

Meanwhile, for her column this month, industry expert Dr. Jennie S. Hwang of H-Technologies Group focuses on crystal structure and defects—a conclusion to her series on the key processes likely engaged in tin whisker growth.

In the second part of his column series, Michael Ford of Mentor Graphics covers material management, and how Lean supply-chain logistics are an essential component of a "smart factory."

Next, we have Tom Borkes of The Jefferson Project writing about the role of leadership in your company.

At the recent SMTA International 2016 event, my colleague Patty Goldman caught up with Joe Russeau, president of the Precision Analytical Laboratory, to discuss a paper he presented at the conference. Co-authored by Mark Northrup and Tim Estes, "Chemical Data vs. Electrical Data: Is One a Better Reliability Predictor?" presents early data comparing the results of two different analytical test methods to determine how well they correlate with each other as predictors of PCB cleanliness and reliability.

Meanwhile, we bring you an interview I conducted with James Liu, director of Standardization and Electronics Manufacturing at the Smart Factory Institute of the China Science and Technology Automation Alliance (CSAA). He discusses how the alliance is helping the small- and medium-sized companies in China make their factories smarter.

We also feature China-based editor Edy Yu's interview with Daniel Chan, executive director of the Hong Kong Printed Circuit Association (HKPCA), and Helen Guo, Member Service Director of IPC Greater China. They share some of the new features and highlights of the upcoming show, including the popular Hand Soldering Competition. The International Printed Circuit & APEX South China Fair will be held December 7–9 in Shenzhen, China.

I hope you'll enjoy this month's issue of *SMT Magazine*. Next month, we will look into the challenges for sales and marketing executives in the PCB assembly industries, highlight the key attributes of a sales person, and provide effective sales strategies to use to be successful in this industry. **SMT**

Stephen Las Marias is managing editor of *SMT Magazine*. He has been a technology editor for more than 12 years covering electronics, components, and industrial automation systems.

Millennials in Manufacturing

By Davina McDonnell, Saline Lectronics

Most of you have heard of the concern about the manufacturing skills gap—how baby boomers will soon start retiring from manufacturing careers with no one to replace their vacancies. Most news stories and studies present this as a major crisis—millennials simply aren't interested in manufacturing careers and if we don't do something about it, well, American manufacturing as we know it will disappear.

Here's the thing. I'm a millennial in manufacturing. I work for an electronics manufacturing company with a workforce that's almost 50% Millennial. Within Saline Lectronics, there's no crisis. As I walk the production floor, I am surrounded by young, eager faces who seem happy and keenly interested in their manufacturing jobs.

Based on my observations, millennials are very enthusiastic about their manufacturing careers, but it wasn't until they were working in manufacturing that they understood the opportunities available within the industry. Prior to that, their perception of a manufacturing career wasn't very positive.

From my perspective, the manufacturing industry isn't accurately represented in the media, or in school, as a viable career path; therefore, struggles to connect with younger generations persist. Many initiatives aren't resonating, or even reaching, the intended audience.

If we're truly concerned about filling the skills gap, it's time to re-examine how manufacturing is being presented to the younger generations. Instead of hoping these generations will adapt to the industry, it's time for the image of manufacturing to adapt to millennials.

Editor's Note: New columnist Davina McDonnell will be writing on the challenges millennials face in the workplace, and the unique dynamic between millennials and the industry veterans who manage them.

The Theory Behind Tin Whisker Phenomena, Part 5

by Dr. Jennie S. Hwang
H-TECHNOLOGIES GROUP

In this installment of the series, we will complete the discussion of key processes likely engaged in tin whisker growth. These key processes include:

1. Grain boundary movement and grain growth
2. Energy dynamic of free surface
3. Role of recrystallization
4. Solubility and grain growth in response to external temperature
5. Lattice vs. grain boundary diffusion
6. Reaction and dynamic of intermetallic compounds
7. Crystal structure and defects

In Parts 2, 3, and 4, we discussed the first six; now we will outline the last processes for crystal structure and defects.

Crystal Structure and Defects

Crystal structure is the bedrock of properties and behavior of materials.

Crystal structure defects and the dynamics of defects including dislocation structure and its movements account for the characteristics and performance of materials. Because the stress needed to move dislocations increases with the spacing between the planes, dislocations are expected to move along the densest planes of atoms in a material. Let's take two primary parameters of crystal lattice into consideration: type of unit cell and atomic packing factor (APF).

Face-centered cubic (FCC) and body-centered cubic (BCC) metals have more dense planes than other crystal structures, so dislocations move relatively easy and the materials possessing these crystal structures impart

high ductility. Lattice structures with closely packed planes allow more plastic deformation than those that are not closely packed. It is easier for planes of atoms to slide by each other if those planes are closely packed. For example, lead (Pb) with FCC lattice structure exhibits higher ductility than tin (Sn) with tetrahedral lattice. However, when obstacles are introduced into the lattice structure, such as interstitial atoms or grain boundaries, dislocations can be pinned and their movements hindered. In addition, if more dislocations are produced they will get into each other's way and impede their own movements.

Within cubic lattice, a FCC crystal structure will exhibit more ductility (deform more readily under load before breaking) than a BCC structure. The BCC lattice, although cubic, is not closely packed and forms strong metals (e.g., alpha-iron and tungsten). The FCC lattice is both cubic and closely packed and forms more ductile materials (e.g., silver, gold, and lead).

Comparing between cubic-lattice (FCC, BCC) and non-cubic lattice (HCP, tetragonal, orthorhombic, monoclinic) structures, cubic-lattice structures allow slippage to occur more easily than non-cubic lattices because their symmetry provides closely packed planes in several directions.

In comparison, hexagonal close packed (HCP) lattices are closely packed, but not cubic. HCP metals (e.g., cadmium, cobalt and zinc) are not as ductile as the FCC metals. The FCC and HCP structures both have an APF of 0.74 and a coordination number of 12, consisting of closely packed planes of atoms (vs. APF of BCC = 0.68). The difference between the FCC and HCP is the stacking sequence. The HCP layers cycle among the two equivalent shifted positions whereas the FCC layers cycle between three positions.

So how does crystal structure affect tin whisker?

Tin possesses a non-cubic crystal structure (tetragonal), thus it does not allow agile slippage to readily occur and cannot proceed deformation easily. Indium also has a tetragonal crystal structure. This "inconvenient slippage" contributes to the driving forces in forming whiskers. Zn has a HCP structure. Comparing Sn with Zn, Sn's lower APF (0.54) further facilitates whisker process as the result of more free diffusion distance, thus it is expected that Sn is even more prone to whisker than Zn.

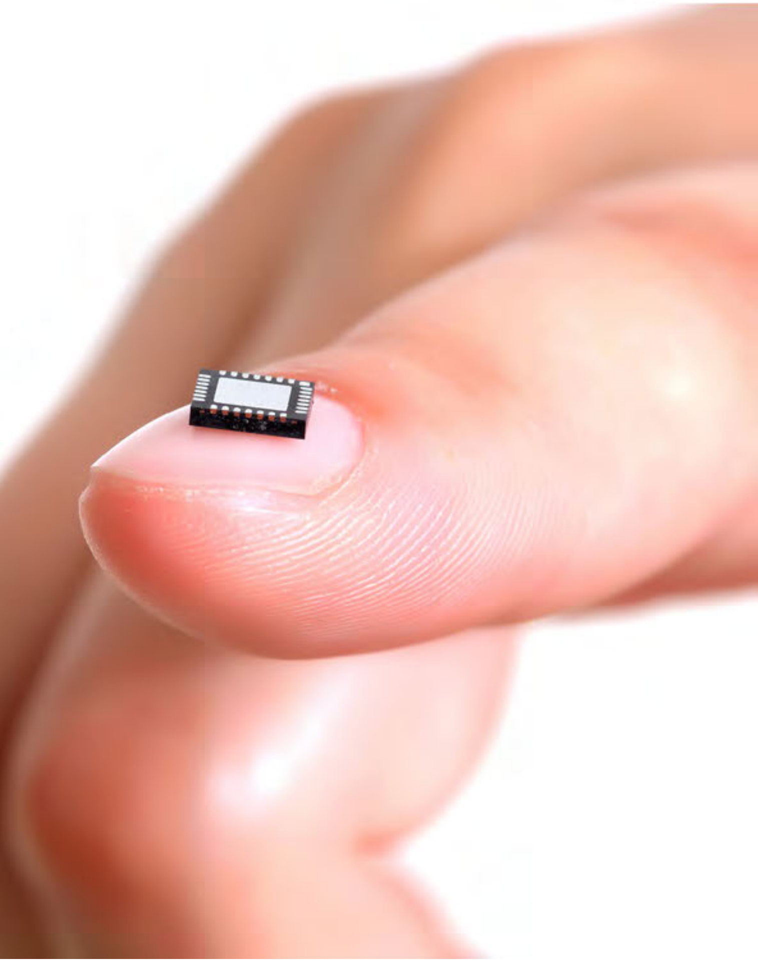
From crystal structural perspective, among the common metals used in electronics, what is the relative whisker propensity?

If the role of crystal structure is a pure play in whisker process, tin and indium are more prone to whisker than zinc. In turn, Zn is more prone to whisker than Pb, Ag, Au and Cu.

Part 6 will conclude the series by summarizing the theory behind tin whisker phenomena. **SMT**

Dr. Hwang is a forward thinker, an international businesswoman, international speaker, and a business and technology advisor. She is a pioneer of and long-standing contributor to SMT manufacturing since its inception, as well as to the lead-free electronics implementation. Among her many awards and honors are induction into the International Hall of Fame—Women in Technology, election to the National Academy of Engineering, YWCA Women Achievement Award, and being named an R&D-Stars-to-Watch (Industry Week). Having held senior executive positions with Lockheed Martin Corp., Sherwin Williams Co., Hanson, plc, IEM Corp., she is currently CEO of H-Technologies Group, providing business, technology and manufacturing solutions. She serves as Chairman of Assessment Board of DoD Army Research Laboratory, National Institute of Standards and Technology (NIST), National Materials and Manufacturing Board, Board of Army Science and Technology, Commerce Department's Export Council, various national panels/committees, international leadership positions, and the board of Fortune 500 NYSE companies and civic and university boards. She is the author of 450+ publications and several textbooks, and a speaker and author on trade, business, education, and social issues. Her formal education includes four academic degrees (Ph.D., M.A., M.S., B.S.) as well as Harvard Business School Executive Program and Columbia University Corporate Governance Programs. For more information, click here.

The Impact of Via and Pad Design on QFN Assembly



David Geiger, Anwar Mohammed and Jennifer Nguyen*
FLEX

Abstract

Quad flat no-lead (QFN) packages have become very popular in the industry and are widely used in many products. These packages have different size and pin counts, but they have a common feature: a thermal pad at the bottom of the device. The thermal pad of the leadless QFN provides efficient heat dissipation from the component to PCB. In many cases, a thermal via array under the component is used to conduct heat away from the device. However, thermal vias can create more voids or result in solder protrusion onto the secondary side.

This paper discusses our study on the impact of via size and via design on QFN voiding and solder protrusion. Does a small via prevent the solder to flow to the other side? How should the via be designed? Which via type will have less of a voiding issue? A comprehensive experiment was designed to try to answer these questions. Different QFN types, via design, via sizes, via pitches and stencil design were studied using three different board thicknesses: 1.6 mm, 2.4 mm and 3.2 mm.

Introduction

Quad flat no-lead package is designed so that the thermal pad is exposed on the bottom of the component. This creates a low thermal resistance path between the die and the exterior of the package and provides excellent heat dissipation from the component to PCB. Thermal vias in the PCB thermal pad are typically used to conduct the heat away from the device and to transfer effectively the heat from the top copper layer of the PCB to the inner or bottom copper layer or to the outside environment. A cross-section view of QFN and PCB thermal vias is shown in Figure 1.

There are several publications about the PCB layout guidelines for QFN packages requiring thermal vias[1-2]. Some recommend thermal vias in the solder mask defined thermal pad[2] while others place the thermal vias directly on

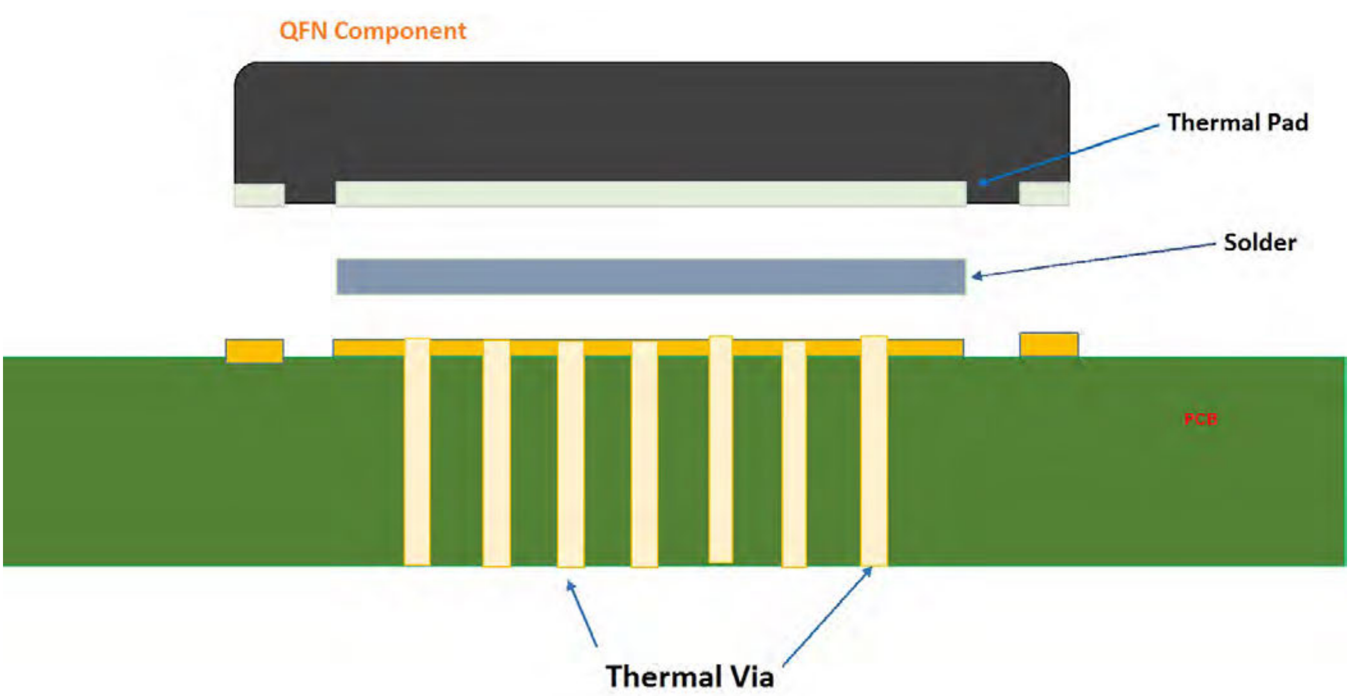


Figure 1: Cross-section of QFN and PCB structure.

the thermal pad without any solder mask[1]. The solder mask around the via can keep the solder away from the via and prevent it from flowing into the via. However, the solder mask ring tends to create more voids or unsoldered areas at the thermal pad. On the other hand, the solder can flow into the thermal vias if there is no solder mask ring and result in solder loss and solder protrusion onto the secondary side, which can interfere with the assembly process and become a quality issue. In this paper, we will discuss the impact of via design, board design and process parameters on solder protrusion at the thermal pad's vias. QFN voiding is a known industry challenge with many publications[3–6]. The influence of via design and processes on voiding will also be presented in the paper.

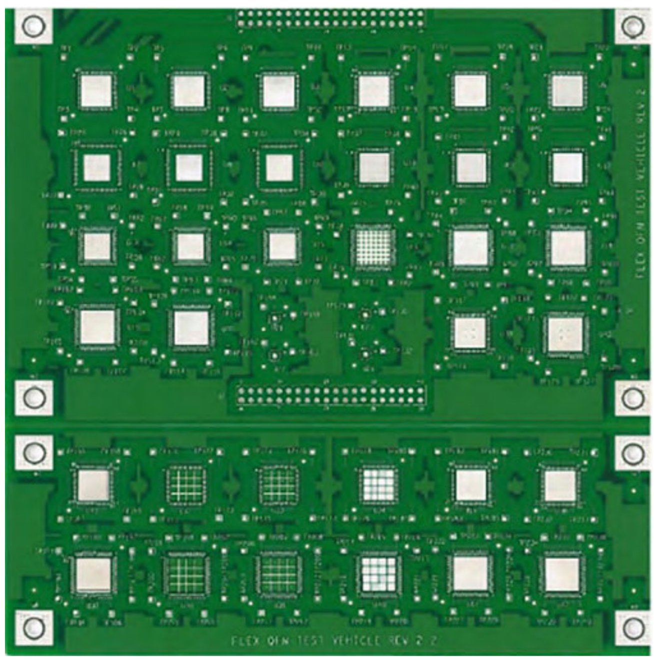


Figure 2: Flex QFN test vehicle Rev 2.

EXPERIMENTAL DETAILS

Test Vehicle and Components

A QFN test vehicle was designed for this study. The test vehicle had the dimension of 177 x 177 mm. The board surface finish was immersion silver (I-Ag). Three different board thicknesses of 1.6 mm (62 mil), 2.4 mm (93 mil) and 3.2 mm (125 mil) were investigated. The image of the test vehicle is shown in Figure 2.

Part ID	P/N	QFN Body Size (mm x mm)	Lead Pitch Outer (mm)	Lead Pitch Inner (mm)	Lead Count
MLF88	A-MLF88-10mm-.4mm	10x10	0.4		88
MLF100	A-MLF100-12mm-.4mm	12x12	0.4		100
MLF68	A-MLF68-10mm-.5mm	10x10	0.5		68
MLF132	A-DualRowMLF132-10mm-.5mm	10x10	0.5	0.65	132
MLF156	A-DualRowMLF-156-12-.5mm	12x12	0.5	0.65	156
MLF16	A-MLF16-3mm-.5mm-DC-Sn-TR	3x3	0.5		16

Table 1: Details of QFN Components.

Via Design Variable	Description
Via Drill Size	8, 9, 10, 12, 20mil
Via Pitch	0.5mm, 1mm, 1.27mm
Via Design	Through-Hole Via with No Solder Mask, Through-Hole Via with Solder Mask

Table 2: Via Design Variables.

Six different QFN packages with different pin counts and component body size were included in the test vehicle. Both single row and dual row QFN components were studied. The QFN pitch varied from 0.4 mm, 0.5 mm to 0.65 mm. The QFN component body size ranged from 3 x 3 mm to 12 x 12 mm. The details of the QFN components is summarized in Table 1.

Design Variables

Many via variables were designed into the test vehicle, including via size, via pitch and via design. Five different via sizes were investigated. They were 0.20 mm (8 mil), 0.22 mm (9 mil), 0.25 mm (10 mil), 0.30 mm (12 mil), and 0.51 mm (20 mil). Via spacing was 0.5 mm, 1 mm and 1.27 mm. Most through hole vias with no solder mask ring were used while some vias were designed with the solder mask around the via. Table 2 summarizes the via design variables.

Process Variables

Besides the component, board thickness and via design variables, the study also included two different stencil designs. Window pane aperture opening and 1:1 pad aperture opening stencils were used. For the window pane design, the solder paste was printed away from the vias except at the 0.5 mm via pitch locations. For the 1:1 pad design, the paste was printed over the vias. The example of the window pane aperture opening is shown in Figure 3. In addition, the boards were reflowed using air and nitrogen, and were reflowed using two different reflow ovens.

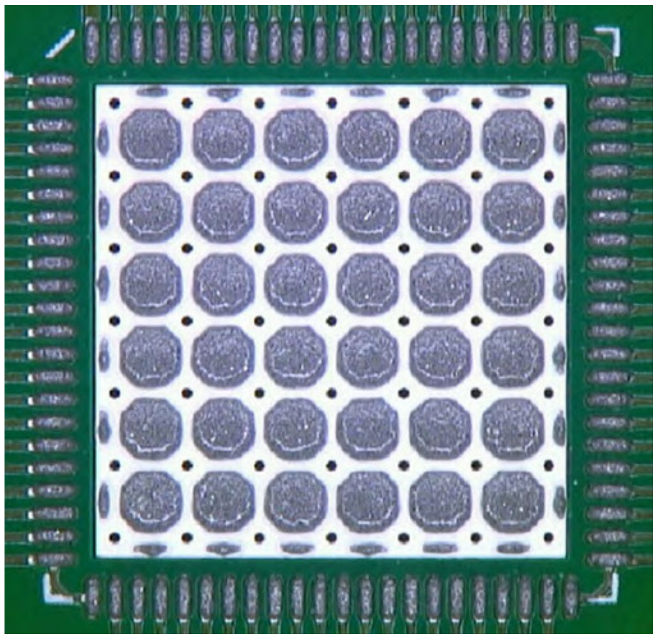
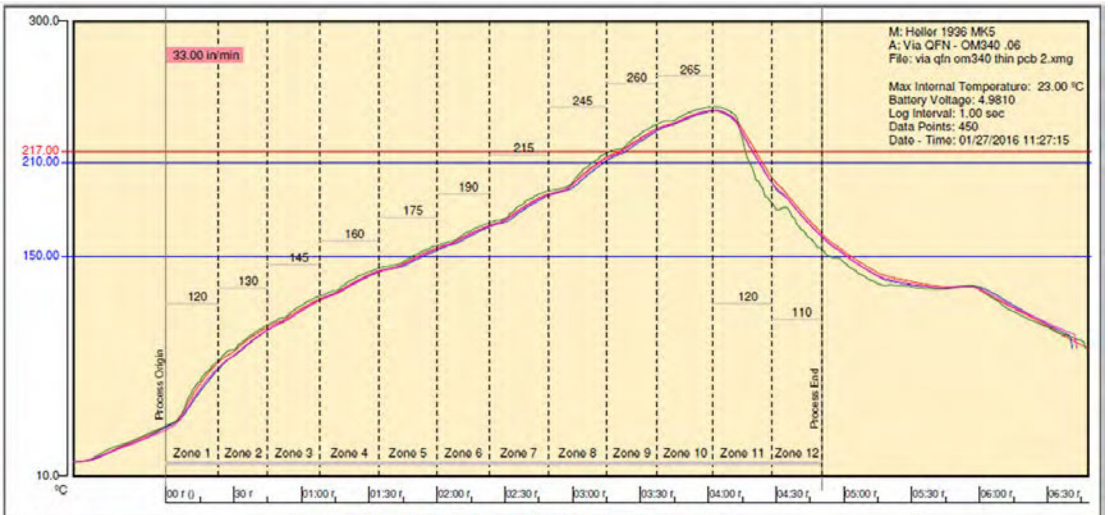


Figure 3: Example of window pane aperture opening.

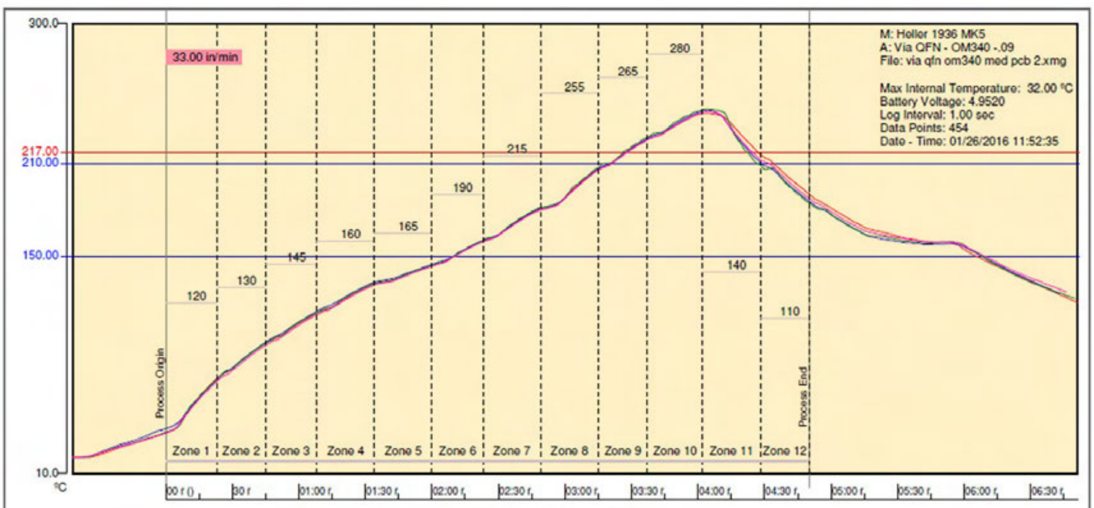
Reflow Profiles

Three similar lead-free reflow profiles were generated for each board thickness. The oven temperature settings were used based on the board thickness. To achieve this, higher oven temperatures were used for thicker board while



		Maximum Positive Slope	Time Between Temperature	Slope: Temperature to Peak	Maximum Temperature	Time Above Temperature : Total (+/-)	Slope: Peak to Temperature
		–0-150–	150-210°C	217-Peak		≥217°C	Peak-217
Show All		°C/sec	sec	°C/sec	°C	sec	°C/sec
A1	U1	2.31	80	0.63	243.0	60	-1.40
A2	U42	2.04	80	0.65	242.8	56	-1.60
A3	U21	2.59	80	0.60	245.5	60	-2.29
A4	U16	2.20	81	0.65	243.3	58	-1.56
	Range	0.55	1	0.05	2.7	4	0.89
	Average	2.285	80.3	0.632	243.65	58.5	-1.712
	Std Deviation	0.2316	0.50	0.0236	1.250	1.91	0.3946

Figure 4: Reflow profile of 1.6 mm thick board.



		Maximum Positive Slope	Time Between Temperature	Slope: Temperature to Peak	Maximum Temperature	Time Above Temperature : Total (+/-)	Slope: Peak to Temperature
		–0-150–	150-217°C	217-Peak		≥217°C	Peak-217
Show All		°C/sec	sec	°C/sec	°C	sec	°C/sec
A1	U1	1.96	78	0.72	242.2	59	-1.01
A2	U42	1.70	78	0.74	244.1	56	-1.41
A3	U21	2.05	76	0.73	244.8	56	-1.55
A4	U16	1.81	77	0.70	243.1	57	-1.35
	Range	0.35	2	0.04	2.6	3	0.54
	Average	1.880	77.3	0.722	243.55	57.0	-1.330
	Std Deviation	0.1556	0.96	0.0171	1.139	1.41	0.2292

Figure 5: Reflow profile of 2.4 mm thick board.

the conveyor speed was kept constant for all the profiles. The actual reflow profiles were similar and had the reflow time of around 60 seconds, the soak time of around 70–80 seconds and the peak temperature between 240° to 245°C. The profiles for 1.6 mm, 2.4 mm and 3.2 mm thick board were shown in Figure 4, 5 and 6, respectively.

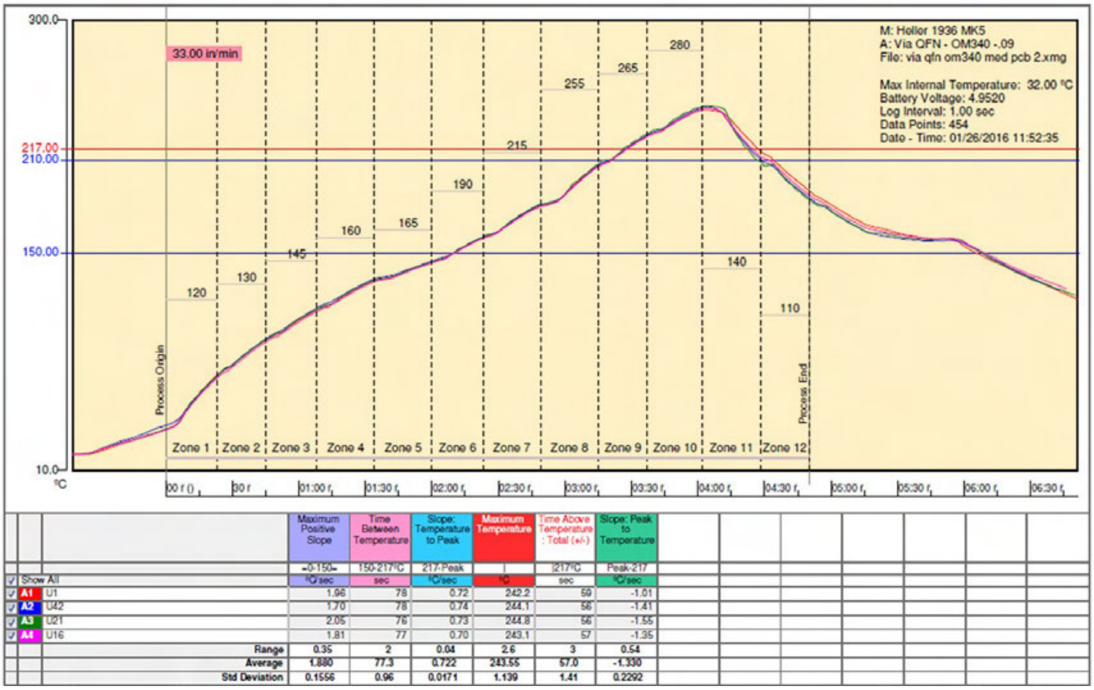


Figure 6: Reflow profile of 3.2 mm thick board.

RESULTS AND DISCUSSION

Via Measurement

The via diameter of different via sizes was measured before the assembly. Both drill size and hole size were measured according to Figure 7.

The measured drill sizes were consistent and close to the theoretical drill sizes. The hole size was smaller than the drill size. It was expected because of the copper plating at the via. The drill size measurements of different board thicknesses are shown in Tables 3-5, and the actu-

Drill Size Measurement_ 62mil Thick PCB	U1	U2	U3	U4	U43
Theoretical Drill Size	[10mil]	[9mil]	[8mil]	[12mil]	[20mil]
1	9.9	8.91	7.4	11.97	19.13
2	9.98	8.95	7.48	11.89	19.21
3	10.06	8.71	7.68	11.65	
4	9.82	8.47	7.52	11.73	
5	9.9	9.03	7.75	11.53	
6	9.82	8.87	7.12	11.69	
7	9.86	8.99	7.68	11.77	
Average	9.91	8.85	7.52	11.75	19.17
STDEV	0.09	0.20	0.22	0.15	0.06

Table 3: Drill size measurement for 1.6 mm thick board.

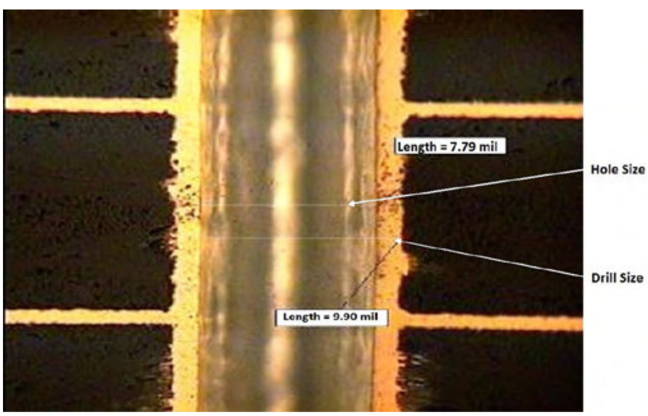


Figure 7: Drill size and hole size definition.

Drill Size Measurement_ 93mil Thick PCB	U1	U2	U3	U4	U43
Theoretical Drill Size	[10mil]	[9mil]	[8mil]	[12mil]	[20mil]
1	10.1	8.83	7.99	11.81	18.73
2	9.9	8.91	7.87	11.85	18.53
3	10.02	8.91	7.95	11.25	
4	9.9	8.75	7.83	11.49	
5	9.94	8.91	7.87	11.45	
6	9.94	9.19	7.6	11.49	
7	9.94	9.11	7.95	12.01	
Average	9.96	8.94	7.87	11.62	18.63
STDEV	0.07	0.15	0.13	0.27	0.14

Table 4: Drill size measurement for 2.4 mm thick board.

Drill Size Measurement_ 125mil Thick PCB	U1	U2	U3	U4	U43
Theoretical Drill Size	[10mil]	[9mil]	[8mil]	[12mil]	[20mil]
1	10	9.24	8.03	12.17	19.81
2	10.12	9.08	7.99	12.13	19.44
3	10	9.08	8.24	12.21	
4	10.04	9.16	8.07	12.05	
5	9.88	9	8.28	11.93	
6	9.88	8.92	8.16	11.89	
7	9.96	8.88	8.24	11.89	
Average	9.98	9.05	8.14	12.04	19.63
STDEV	0.09	0.13	0.12	0.14	0.26

Table 5: Drill size measurement for 3.2 mm thick board.

Actual Hole Size Measurement_ 1.6mm Thick PCB	U1	U2	U3	U4	U43
Theoretical Drill Size	[10mil]	[9mil]	[8mil]	[12mil]	[20mil]
1	7.79	6.76	5.21	9.58	16.5
2	7.68	6.8	5.29	9.58	16.8
3	7.79	6.56	5.69	9.27	
4	7.64	6.2	5.33	9.35	
5	7.72	7	5.65	9.27	
6	7.56	6.72	4.85	9.31	
7	7.4	6.88	5.53	9.5	
Average	7.65	6.70	5.36	9.41	16.65
STDEV	0.14	0.26	0.29	0.14	0.21

Table 6: Actual hole size measurement for 1.6 mm thick board.

Actual Hole Size Measurement_ 2.4mmThick PCB	U1	U2	U3	U4	U43
Theoretical Drill Size	[10mil]	[9mil]	[8mil]	[12mil]	[20mil]
1	7.04	5.61	5.21	9.03	15.67
2	6.84	5.73	4.85	9.11	15.59
3	7	5.81	5.05	8.19	
4	7.08	5.49	5.09	8.59	
5	7.16	5.73	4.97	8.55	
6	7.08	6.12	4.45	8.59	
7	6.84	6.28	4.97	9.07	
Average	7.01	5.82	4.94	8.73	15.63
STDEV	0.12	0.28	0.24	0.34	0.06

Table 7: Actual hole size measurement for 2.4 mm thick board.

Actual Hole Size Measurement_ 3.2mm Thick PCB	U1	U2	U3	U4	U43
Theoretical Drill Size	[10mil]	[9mil]	[8mil]	[12mil]	[20mil]
1	5.42	4.86	4.06	7.47	14.7
2	5.74	4.86	4.02	7.59	14.26
3	5.62	6.55	4.66	7.71	
4	5.7	4.98	5.5	7.59	
5	5.34	4.42	4.14	7.35	
6	5.34	4.7	4.26	6.99	
7	5.42	4.26	5.91	7.39	
Average	5.51	4.95	4.65	7.44	14.48
STDEV	0.17	0.75	0.76	0.24	0.31

Table 8: Hole size measurement for 3.2 mm thick board.

al hole size measurements are shown in Tables 6-8, respectively.

Impact of Via Design on Solder Protrusion

Solder flow down to the via was seen for all the PTH via sizes tested in this study. Solder protrusion onto the secondary size was seen for most of the via sizes with no solder mask ring. 0.2 mm (8 mil) via with the actual hole size of ~ 0.10–0.13 mm (4-5 mil) hole didn't eliminate solder protrusion. More solder protrusion was seen for smaller via sizes. On the other hand, 0.51 mm (20 mil) via with window pane stencil design resulted in no solder protrusion for 1.6 mm and 2.4 mm thick boards. Thicker boards didn't prevent the solder protrusion onto the secondary side. In fact, solder protrusion onto the secondary side was seen at 0.51 mm (20 mil) via of a 3.2 mm thick board. It was probably because the higher oven temperature setting of the 3.2 mm thick board allowed the solder to spread more than the lower temperature settings used for the thinner boards. The solder images of different via sizes at the secondary side of 1.6 mm thick, 2.4 mm thick and 3.2 mm thick boards are shown in Figures 8, 9 and 10 respectively.

The solder mask ring helped to prevent the solder from getting into the via. No solder protrusion was seen in the via designed with the solder mask ring for 12 mil via using window pane stencil design, as shown in Figure 11.

Impact of Via and Pad Design on Voiding

On the contrary, the through hole via with the solder mask ring showed more voiding area as compared to the through hole via with no solder mask ring (Figure 12). Voiding difference due to different via size was insignificant (Figure 13).

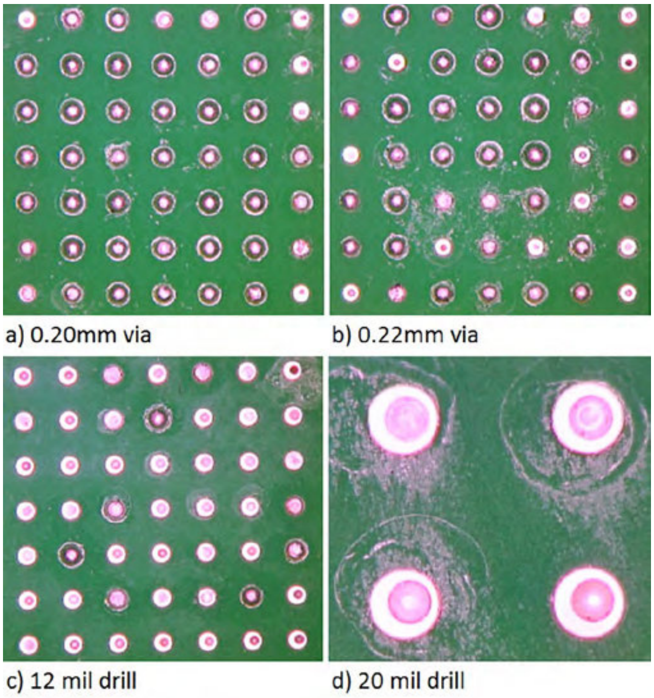


Figure 8: Solder protrusion images for 8, 9, 12, and 20 mil reflowed using 1.6 mm thick board.

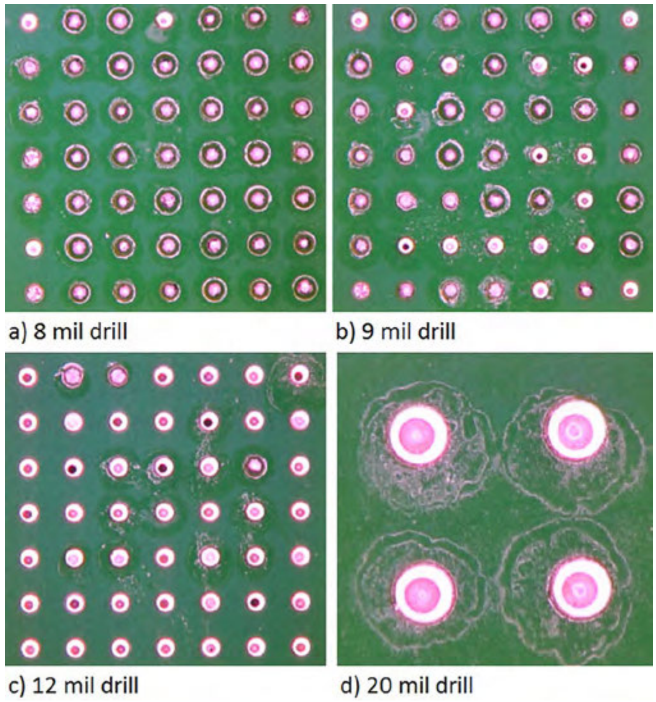


Figure 9: Solder protrusion images for 8, 9, 12, and 20 mil reflowed using 2.4 mm thick board.

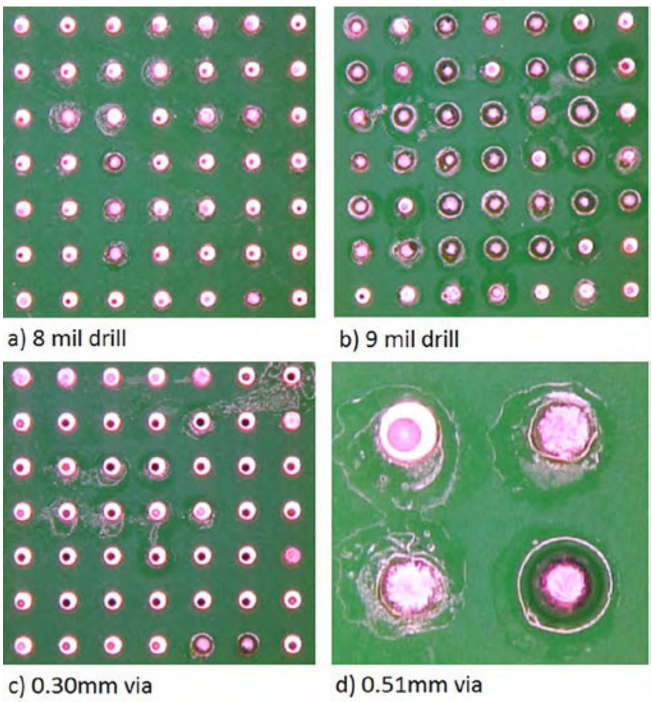


Figure 10: Solder protrusion images for 8, 9, 12, and 20 mil reflowed using 3.2 mm thick board.

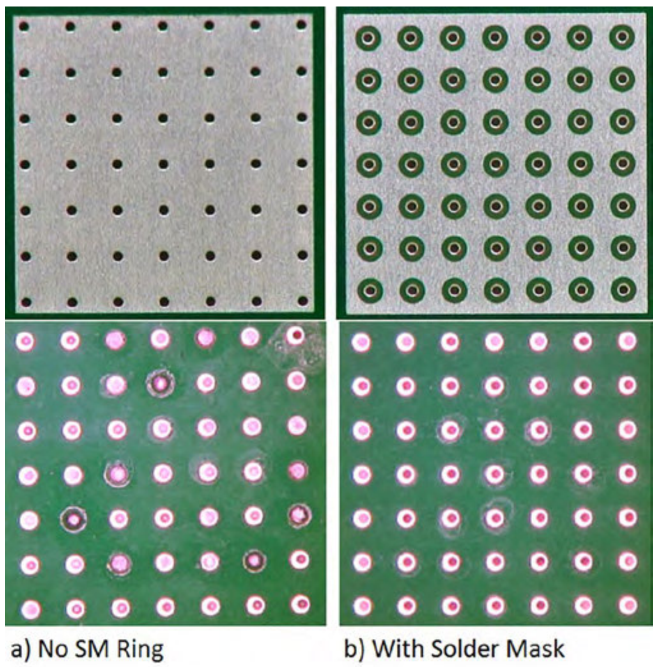
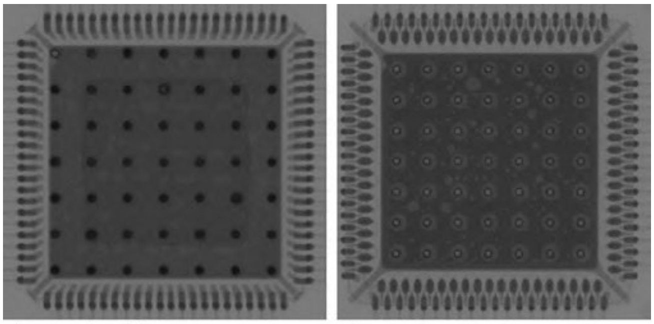
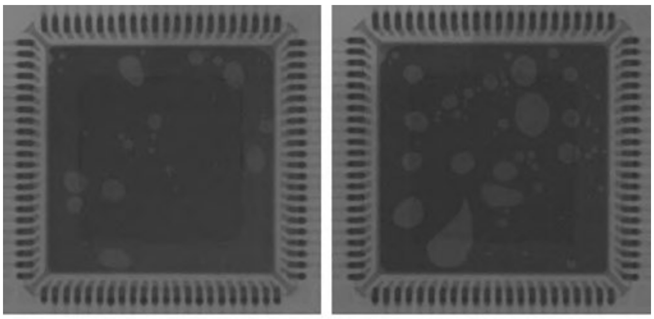


Figure 11: Visual images of solder at the secondary side for through hole via with no solder mask and for through hole via with solder mask ring around the via.



a) PTH via with no SM b) PTH via with SM

Figure 12: X-ray images of QFN with no solder mask ring around thermal via and with the solder mask ring around the thermal via. a) PTH via with no solder mask, b) PTH via with solder mask ring.



a) No via b) Via in pad

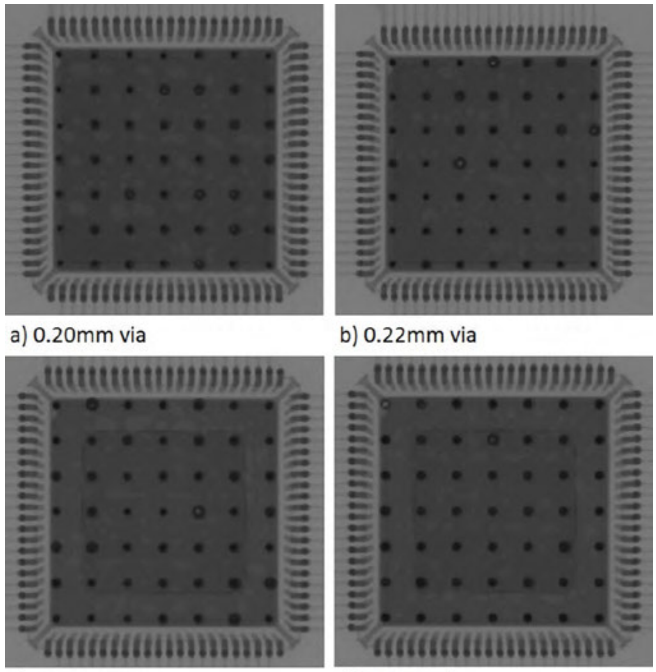
Figure 14: Voiding images of QFN thermal pad with no via, and with via in pad.

The study showed that PTH via resulted in less voids and smaller voids than no via and via in pad. It was because PTH via created a channel for air outgassing during the reflow and solder joint formation. The voiding X-ray images of the thermal pad designed with no via and via in pad are shown in Figure 14.

Breaking the large thermal pad into smaller pads resulted in smaller voids. However, the overall void percentage didn't decrease significantly (Figure 15).

Impact of Board Thickness and Component Type

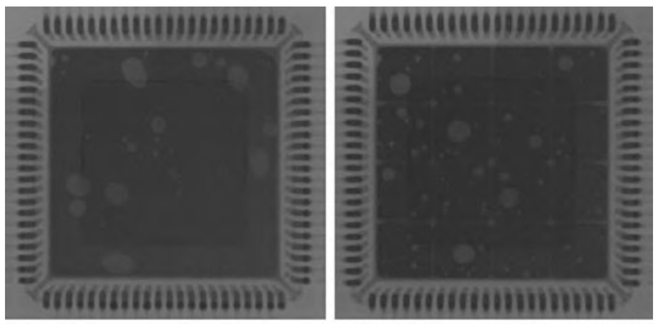
QFN package design played a critical role in voiding formation of the solder joint. The data showed that dual row QFN resulted in more voiding than the single row QFN component.



a) 0.20mm via b) 0.22mm via

c) 0.25mm via d) 0.3mm via

Figure 13: Impact of via size on voiding.



a) One large thermal pad b) Multiple smaller thermal pad

Figure 15: X-ray images of voiding at large pad vs. small pads.

Similar QFN type, but different package design, would result in different voiding level, as shown in the case of QFN132 and QFN156 (Figure 16). Thicker boards didn't result in more voids or less solder protrusion with a similar profile (Figure 16), but higher temperature and hotter profile resulted in more voids (Figure 17).

Impact of Assembly Process on Voiding

In general, slightly more voids and bigger voids were seen when temperature increased.

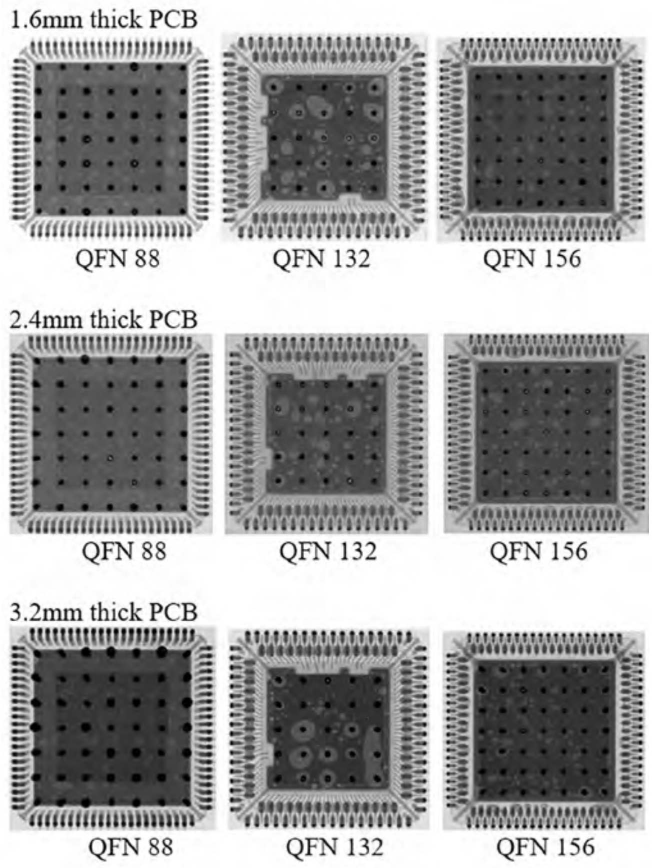


Figure 16: Impact of board thickness and package type on voiding.

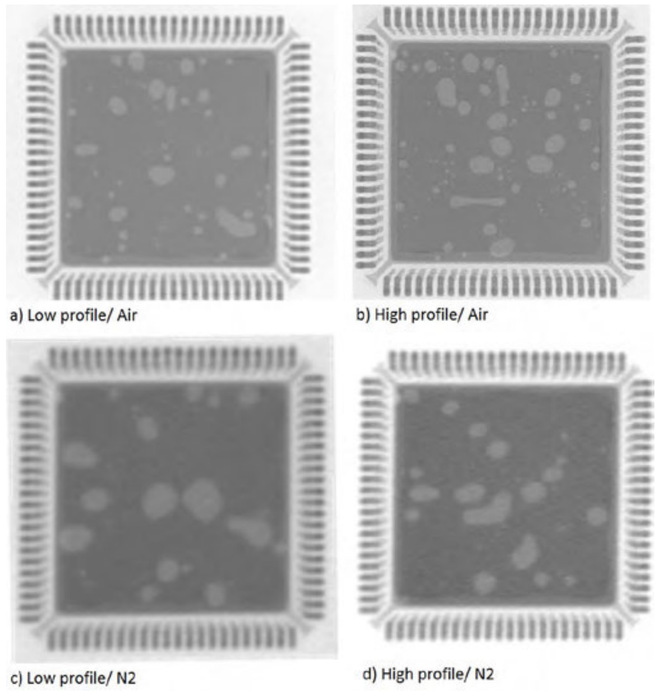
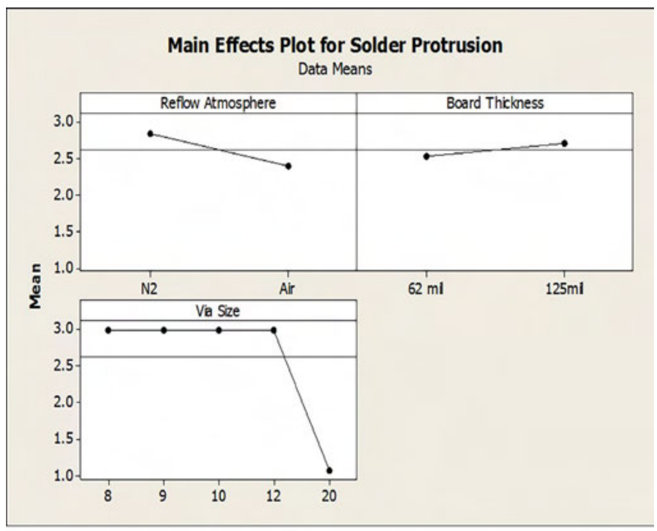


Figure 17: Reflow temperature and atmosphere impact on voiding QFN88. a) low profile in air; b) high profile in air; c) low profile in N2; d) high profile in N2.

Figure 17 shows the voiding of a QFN component reflowed at low and high temperature using air and nitrogen reflow. Smaller voids were observed with air reflow, and less voiding was seen with higher temperature profile. This phenomenon is opposite to the BGA voiding in which less voiding is seen with nitrogen reflow and lower temperature.

Impact of Assembly Process on Solder Protrusion

The main effects plot for solder protrusion from samples reflowed in air and nitrogen environment is shown in Figure 18. The data showed that less solder protrusion was seen when the sample was reflowed in air as compared to nitrogen atmosphere. One explanation is that the solder didn't spread as much in the air atmosphere and resulted in less solder flowing into the via.



Source	DF	Seq SS	Adj SS	Adj MS	F	P
Reflow Atmosphere	1	0.9374	0.9374	0.9374	6.72	0.027
Via Size	4	11.7658	11.7658	2.9414	21.09	0.000
Reflow Atmosphere*Via Size	4	3.7498	3.7498	0.9374	6.72	0.007
Error	10	1.3944	1.3944	0.1394		
Total	19	17.8475				

S = 0.373423   R-Sq = 92.19%   R-Sq(adj) = 85.15%

Figure 18: Impact of reflow atmosphere on solder protrusion.

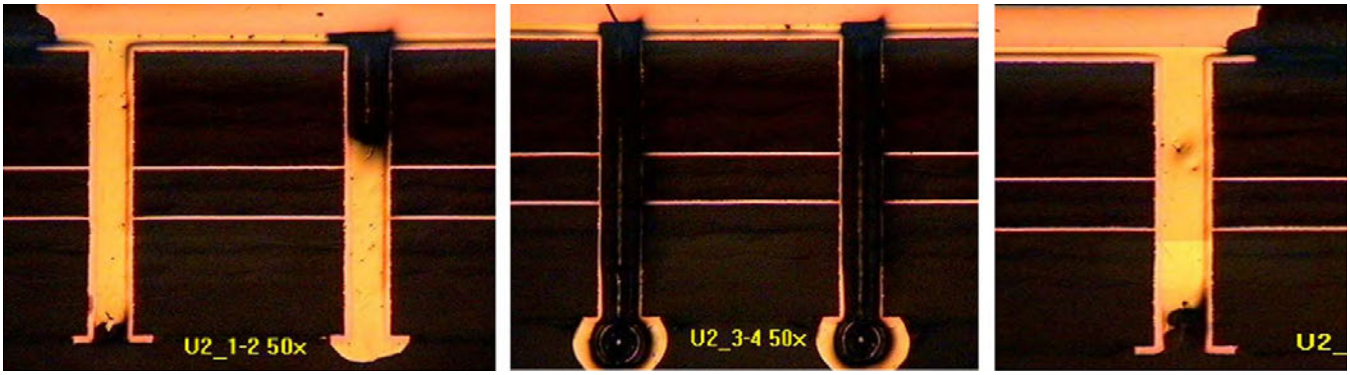


Figure 19: The cross-section of 0.22 mm (9 mil) via using 1.6 mm thick PCB.

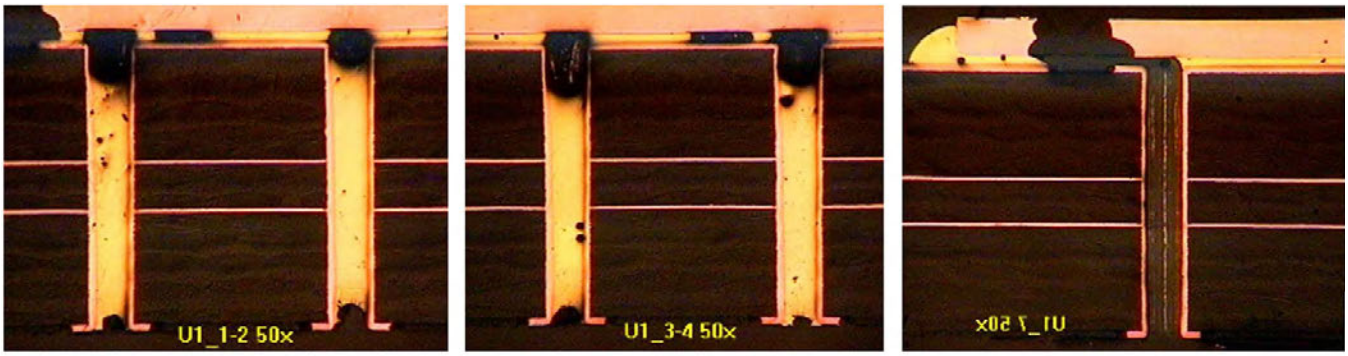


Figure 20: The cross-section of 0.25 mm (10 mil) via using 1.6 mm thick PCB.

Cross Sections

Cross-section images showed that vias at the middle of the thermal pad typically had more voids as compared to the vias located closer to the edge of the pad. It was expected because the edge of the component thermal pad would allow more air to be outgassed. The cross-section also revealed the outgassing mechanism and how it would affect solder protrusion. As the solder melted and spread, it would get into the via and fill a portion of the via. The outgassing of the air bubble would push the solder into the via and flow onto the secondary side or expand the existing air gap (void) in the via. Figure 19 and Figure 20 showed the cross-section images of 0.22 mm (9 mil) via and 0.25 mm (10 mil) vias from 1.6 mm thick boards. Figure 21 showed the cross-section images of a 0.25 mm via using a 2.4 mm thick board.

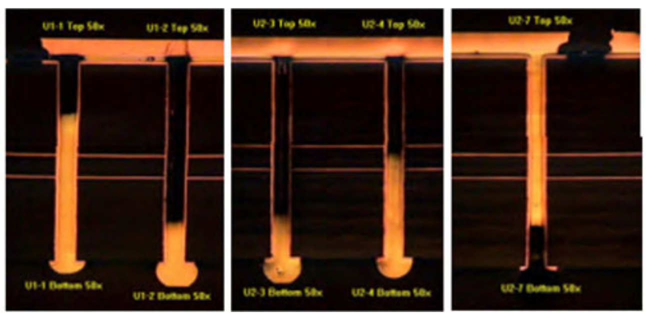
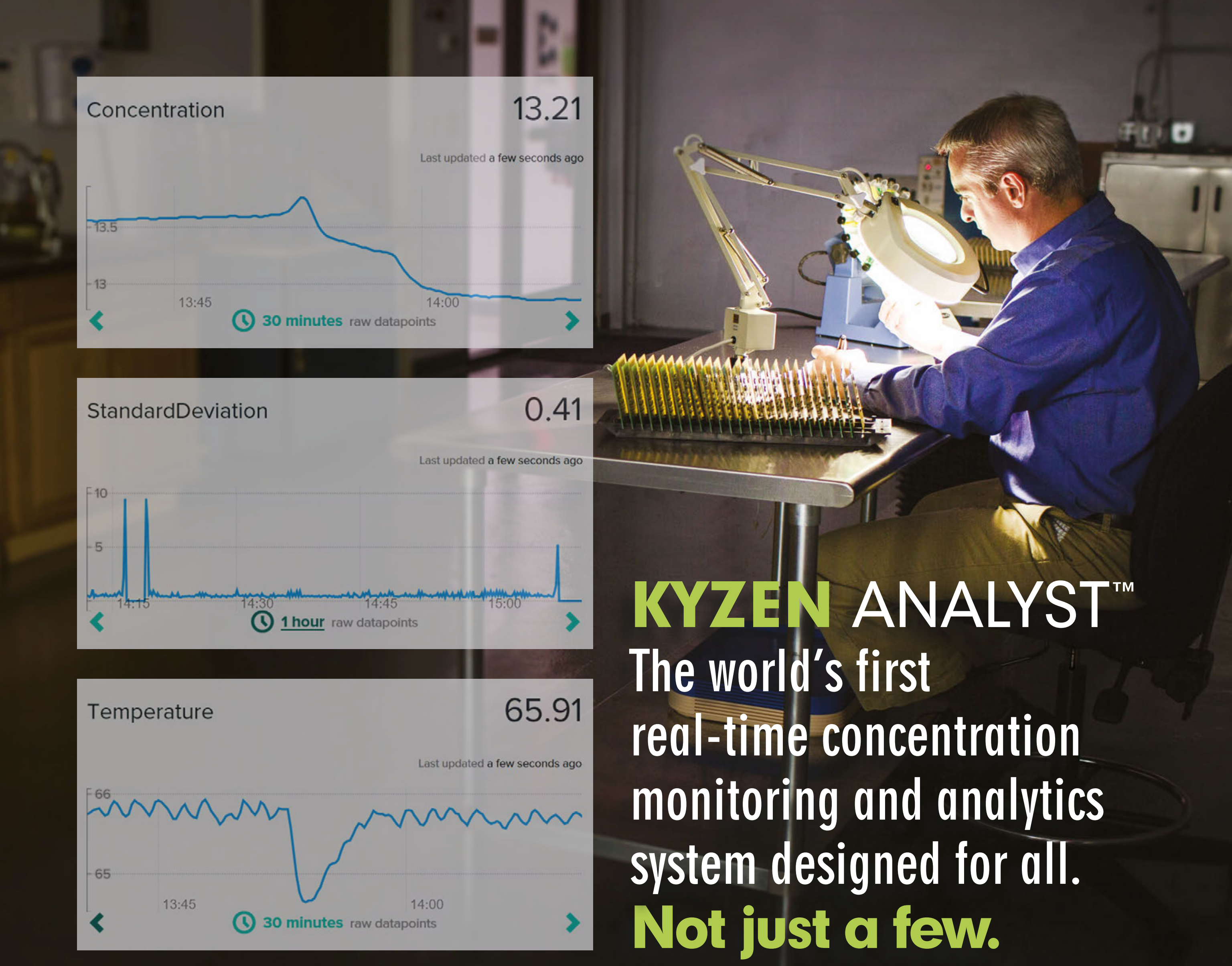


Figure 21: The cross-section of 0.25 mm (10 mil) via using 2.4 mm thick PCB.

Conclusions

Solder was seen flowing into the PTH via with no solder mask ring during the reflow process regardless of the via sizes. The smallest via size was 0.20 mm (8 mil) from the study. Smaller vias didn't result in less solder protrusion on the secondary side. However, less solder protrusion was seen with larger vias. Via size of 0.51 mm (20 mil) with no solder mask ring could result in no solder protrusion, depending on the process condition. Board thickness had no sig-



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nificant impact on the voiding and solder protrusion. Voiding depended more on the component type and design. The solder mask ring would help prevent solder from flowing down the via at the thermal pad. The solder mask ring results in some unsoldered area under the QFN component, which looks like more voiding at the QFN thermal pad.

Acknowledgements

The authors would like to thank Dennis Willie and Robert Pennings at Flex AEG Labs in Milpitas for their help in the assembly. Many thanks to Tu Tran and Francoise Sarrazin at Flex AEG Milpitas lab for the cross-section images. **SMT**

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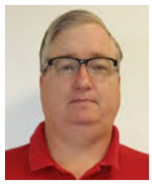


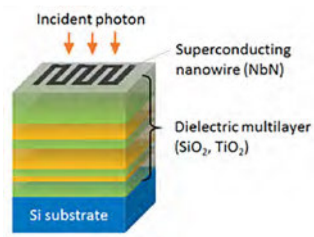
David Geiger is director for assembly and test technology at Flex.

Anwar Mohammed is a senior director at Flex.

***Jennifer Nguyen** left Flex in August 2016.

Flexible Optical Design Method for Superconducting Nanowire Single-Photon Detectors

The National Institute of Information and Communications Technology has succeeded in the development of flexible optical design method for superconducting nanowire single-photon detectors (SSPDs or SNSPDs).



This technique enables SSPDs with a broadband high detection efficiency reject a specific wavelength, and is effective for multidisciplinary applications in fields such as the quantum cryptography, fluorescence spectroscopy, and remote sensing that require high efficiency over a precise spectral range and strong signal rejection at other wavelengths.

This achievement appeared in the Scientific Reports. The reported results have been partially obtained as a part of JST-SENTAN program and AMED-SENTAN program from April 2015.

The developed SSPD with the dielectric multilayer and the optical design method can be applied for wide wavelength region between ultraviolet and mid-infrared, and thus provides an important basis for development of application of SSPD to quantum cryptography, fluorescence spectroscopy, and remote sensing.

In support of the SSPD measurements, the NICT team collaborated with Japan's Osaka University and Scotland's University of Glasgow through the NICT internship scheme.

Supply Lines Highlights

The Blackfox Advanced Manufacturing Program for Military Veterans

The Blackfox Veteran's Training Program is the first program of its kind to provide veterans with little to no industry experience with the skills to grow their careers in the electronic assembly industry.

Real Time with... SMTAI: KYZEN Pushes Cleaning Data to the Cloud

At the recent SMTA International exhibition, Tom Forsythe, executive vice president of Kyzen, discusses with I-Connect007's Andy Shaughnessy their latest system that helps customers have a better handle on their cleaning process.

Alpha Launches New Stencil Technologies at Enova Show in Paris

Alpha Assembly Solutions's tensoRED Master Tensioning Frame is designed to provide a higher and more even tension compared to the ALPHA Tetra Frame.

Cogiscan Partners with Siemens PLM on Industry 4.0 Solutions for Electronics Manufacturing

Cogiscan Inc. is partnering with Siemens PLM Software to provide a complete manufacturing software solution to enable Industry 4.0 for Electronic Manufacturers.

Indium Technology Experts to Present at 2016 EPTC

Indium Corporation's Jason Chou and Kenny Chiong will present at the 2016 Electronics Packaging Technology Conference in Suntec City, Singapore.

Rehm Technology Day: Manufacturing in the Age of Digital Transformation

Rehm Thermal Systems' recent Technology Day featured presentations and interesting workshop sessions that took visitors on a journey through the manufacturing of tomorrow and presented the latest in innovative plant technology and the latest software tools.

KYZEN Partners with Stratus Technologies to Strengthen US Market

KYZEN has partnered with Stratus Technologies to promote, sell and support KYZEN's full range of high-performance cleaning products throughout the United States.

Dymax Receives Marcum Tech Top 40 Award

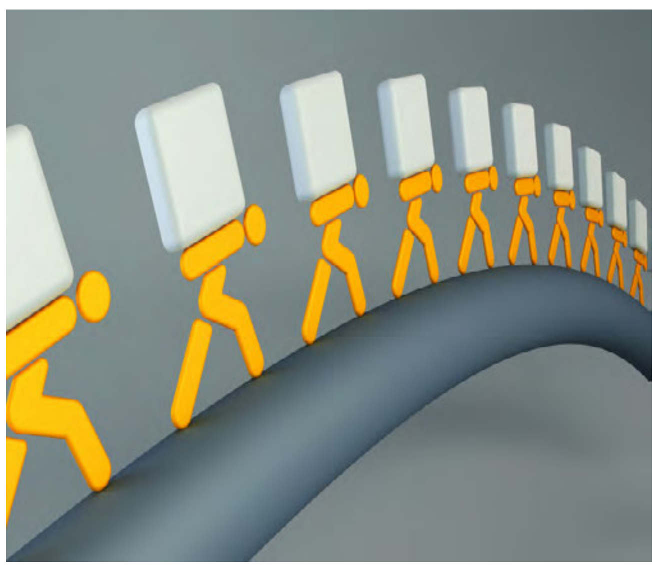
The Connecticut Technology Council and Marcum LLP announced Dymax Corp. has made the Marcum Tech Top 40 list of fastest growing technology companies in Connecticut.

Mycronic Lands Order for Recently Launched FPS6100 Mask Writer

Mycronic AB has received an order for the newly released FPS6100 mask writer within the multipurpose segment from a customer in Asia.

Improved Production Throughput in SPEA Flying Probe Systems through Extension of Boundary Scan Integration

The boundary scan integration in the flying prober 4060 from SPEA is being expanded to the ability of panel test, enabling several boards to be now be tested and also use the whole performance of the interactive test.



FEATURE

The Taken-for-granted Via

by W. Scott Fillebrown
LIBRA INDUSTRIES

Vias are interesting little creatures. They are so simple, yet they can be so complex at the same time. Designed properly, they complete a circuit. However, a poorly designed via can be a reliability nightmare. The bottom line is that, in many ways, they are the unsung hero to a circuit board, much like an offensive line is to a football team.

Historically, we have tried to minimize their use to save money at the bareboard manufacturer. While this is still common practice, there are times extra vias are a good, useful addition to the board. In today's world, standard vias have very little impact on the costing structure. Complex vias, on the other hand, can add cost and potentially decrease the reliability—clearly not the bargain you wanted.

So what are the different types of vias, and why are they complex? First, the types of vias really have not changed. The most typical are standard vias, which are drilled from one side of the board to the other. Then you have your blind via that can be seen only from one side of the board. Finally, you have your "crazy uncle" via that we call the buried via. He is the one we hide in the middle of the board so no one can see him! While each of these vias has been around for a long time, space constraints have caused significant design approach changes to support them through the manufacturing process.

The largest growth area for vias is blind and buried vias. Many of us remember the days when using a blind or buried via was considered a death nail in the cost structure of our bareboard. We did just about anything to avoid using them. A couple of the microvia approaches including laser drilled vias, and via-in-pad made them avoidable a while longer. However, over time, blind and buried vias became unavoidable. While still expensive, their use

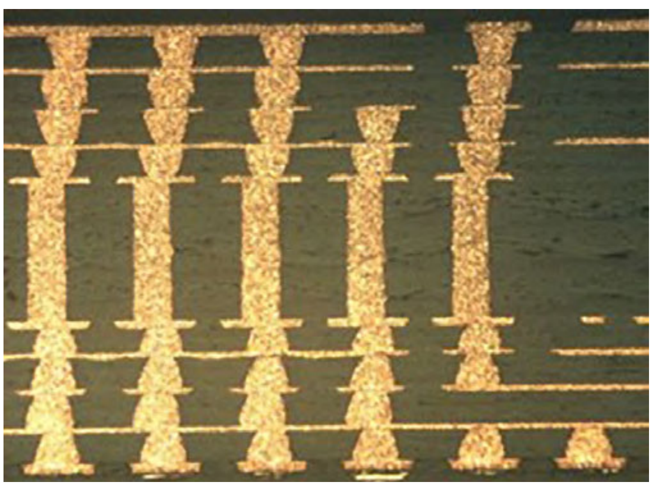


Figure 1: An example of the copper fill process.

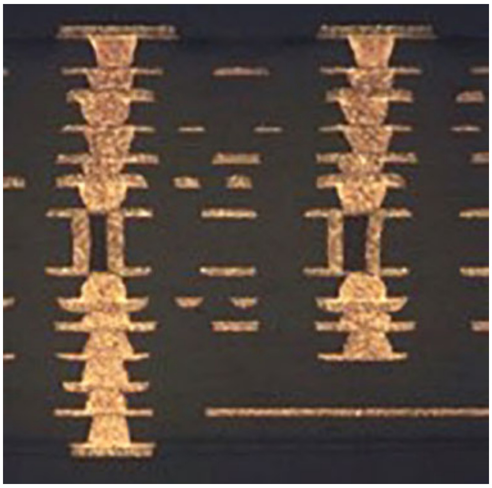


Figure 2: Epoxy fill with copper vias.


Figure 3: Resin fill—stacked vias.


Figure 4: Resin fill—offset vias.

typically is not optional due to space requirements or signal integrity issues. In the past, blind and buried vias required very expensive processes through the board manufacturer, like sequential lamination. However, today there are many approaches to accomplishing blind and buried vias, which have helped reduce the cost of their implantation. A few of these processes include control depth drill, flip drill, stacked via and staggered vias. Each of these methods has their place, and can be reliable when used properly. However, they also can have their drawbacks. The best recommendation is to become best friends with your board manufacturer and rely on their experience to make recommendations for the most reliable and cost-effective approach for your application. Clearly, blind and buried vias still are a more expensive approach and should be avoided if at all possible. Now, regarding their older brother, standard through-the-board vias, could more be better?

When it comes to a standard via, there are times when more can be better. So often we see a via as another hole in the board; however, many times they can be used for more than a conduit from one layer to another. In the R&D process, they can be used for a simple task like probing to diagnose issues or as a point in the circuit to solder a blue wire for engineering changes. While the engineering lab hopefully is a short stay for your board, having additional vias is not just a short-term gain. The biggest gain for having additional vias is for flying probe test. Flying probe is well on its way to being the standard for testing assembled boards in North America. With the advent of dual-sided testers, you have the potential to reach 95% test coverage. Unlike bed-of-nails testers that requires a 30–40 mil test point, flying probe requires a simple via with a 20 mil pad and a 10 mil hole. This approach gives the high-mix, low- to medium-volume manufacturer a viable test approach that supports every company's desire for high quality. The key to taking advantage of these approaches is not to treat them like your crazy uncle, the buried via. You need to be proud of your older brother, the standard via, and not cover them with soldermask. Where the design allows, access is the key to being able to use the via for probing.

Just like the offensive line of your favorite football team, vias get little attention and are taken for granted. But, just as a quarterback is in trouble without a solid offensive line, a circuit board is nothing without a good lineup of vias. It may be time to review your use and design approach for using vias. Are they reliable? Are you getting everything you can out of them? **SMT**

W. Scott Fillebrown is the CTO of Libra Industries. To reach him, click here.

Smart for Smart's Sake, Part 2: Material Management

by Michael Ford
MENTOR GRAPHICS CORPORATION

Data collection in the factory is not just about machine interfaces and gathering data from related assembly processes, it is also about transactional events that directly affect the production operation. In part 2 of this series, we look at how Lean supply-chain logistics are an essential component of a "smart factory," and for good reasons, not least of which are the significant benefits that are brought to the operation.

Last time, we looked at how added-value is created by the normalization of data collected from all machines and processes in the factory, as applied to asset utilization, productivity, visibility, and operational improvement. Whatever we each choose to call this digital revolution in electronics manufacturing, it is actually quite familiar for the old-school industrial engineers among us. It is not just "smart for smart's sake," because real ROIs are created that provide business success and opportunity. Does this ROI still hold true, however, when we look at material management? This is where the "old-school" could learn some new tricks.

The term "material management" is probably one of the most misused terms in the industry because it has been applied to a range of technologies and solutions, from the simple storage of materials in a generic warehouse to fully featured and automated Lean material-logistics solutions.

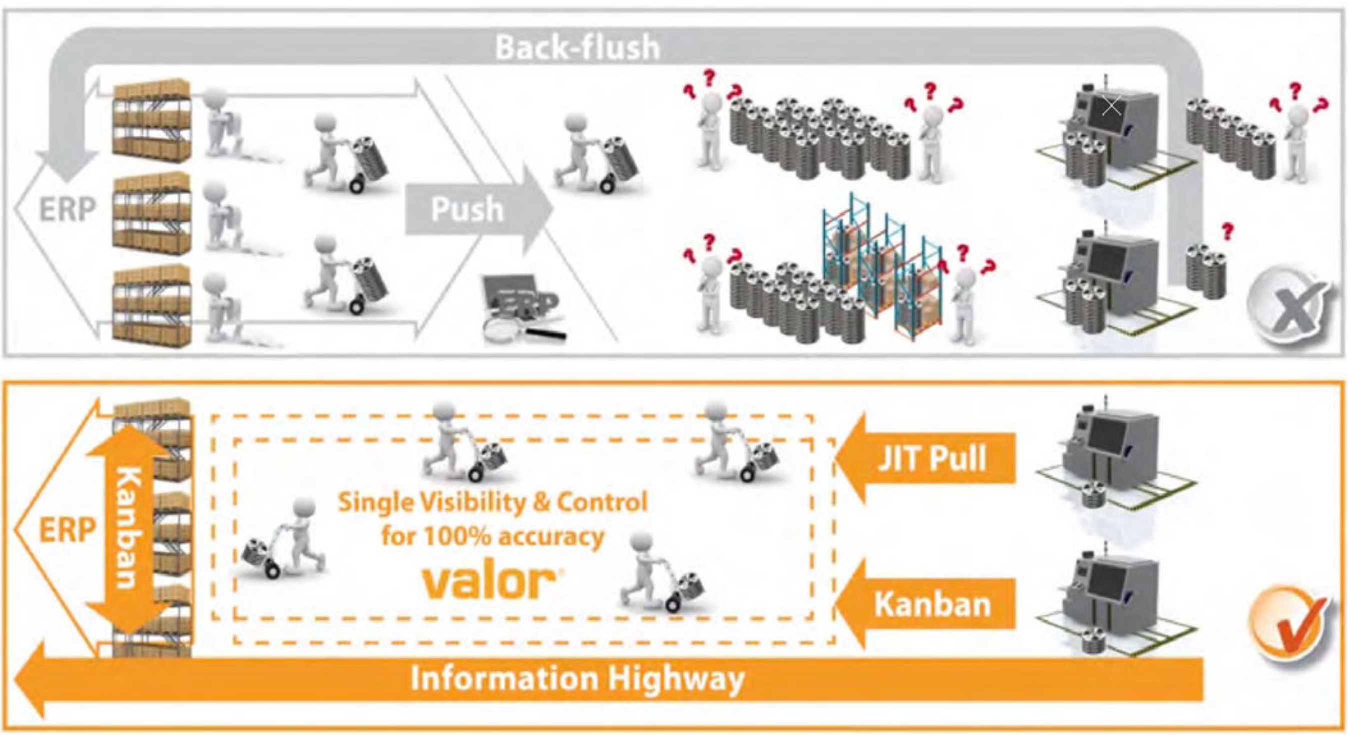
We will need to start at the beginning, where incoming materials are received and logged into the enterprise resource planning (ERP) system, to understand the evolution of material management. ERP management is ultimately responsible for the whole factory inventory, and they will use material requirements planning (MRP) as the tool to order materials based on requirements calculated from the factory production plan and current stock levels. ERP needs to decrement materials while they are used to be able to maintain stock level information, which, in the traditional model, is as products are completed ready for shipping either to the customer or to the next significant internal factory process, referencing the associated bill of material.

This seemingly simple process is complex for electronics, especially in SMT production. Materials are over-supplied to production where they are then only partially used because most materials are on carriers, such as reels. Many opportunities exist for attrition throughout the material setup process on the machines and during the machine operation. Unaccounted material creates inaccurate inventory levels within ERP, which leads to unexpected internal material shortages. This situation occurs quickly and is a serious problem for operations with a higher product mix. Because ERP holds increasingly inaccurate representations of inventory, large buffer stocks have to be maintained and a regular physical stock-check has to be performed to prevent unexpected internal material shortages, both of which are expensive processes for the manufacturing operation.

Even the simplest task of putting materials away in the warehouse can lead to problems. For a warehouse to be successfully managed, the space has to be fully utilized, while ensuring that people can easily and quickly find materials when needed. The easiest way to manage warehouse locations is by part number, which is fine for the ERP managers because they only then need to record within the system the general area in which the materials are stored, which may even be just the warehouse name. Materials are physically easy to find if they are stored in locations that are managed alpha-numerically by part number.

Unfortunately, this is inefficient from a space-usage perspective because storage volume requirements for each part number differ depending on the material size, and the quantity needed for each can fluctuate significantly. New part numbers and end-of-life materials can create significant physical issues for reorder material locations, with associated handling issues. Using "random locations" is far more efficient because each location can be used to their maximum capacity for a greater amount of time, where any location can be used for any material.

The issue then is remembering where the materials are. Where the materials are placed must be recorded, and each "carrier" of materials, such as a reel, needs to be managed using a unique ID, which usually is just a simple barcode created and applied when material is received into ERP. Logistics tasks typically require a mobile barcode reader, which is a little extra



work for materials operators. A computer system is needed to manage the database of materials and their locations, which most often is not practically supported within ERP. The materials-management functions in the manufacturing execution system (MES) can provide supporting warehouse management or even can be the dedicated warehouse management software.

The use of material carousels creates automated and managed storage locations that are efficient on space. These still require reading the material barcodes into the storage, but at least the need to remember the locations is avoided. The units, where big enough, can exist as a named warehouse as far as ERP is concerned. The limitation with the use of carousels is the time that it takes to get materials into and out of the carousel, which often becomes a bottleneck for the operation. However, another benefit of some carousels is that they offer a dry environment for materials, so that baking and separation of moisture-sensitive materials into dry-store locations is unnecessary. Automated carousels cannot be used for all materials, however, especially the larger assembly items and so, in practice, the carousel system in almost all cases has to coexist within a larger overall material management system.

The first part then of our smart solution is to manage material locations, potentially in multiple warehouses, ensuring that no materials are lost, that good use is made of space, and that materials logistics are managed efficiently.

As well as coming into the warehouse, materials also have to leave the warehouse to be used in production. The old-school method of doing this is to prepare a kit of materials well in advance of the product changeover on the line. Preparing material kits has two challenges. The first is to locate the materials, which our "smart" warehouse location system should solve, but the other issue is that there are often not enough materials available. This can be caused by the oversupply of materials to the shop-floor in other kits, as well as the material spoilage, or attrition of material, accumulated over time, for which the additional buffer stocks have been exhausted.

Because this is a frequent occurrence, with a serious effect on production, preparing kits well in advance is a common practice. Often, in higher mix environments, an entire line of material kits will be prepared in advance for each line. The cost of this legacy practice is ridiculously high; for example, the investment in excess material buffer stock, the stock held in queued kits, the workload to create and maintain multiple kits (because often materials are requisitioned from one kit to another), the space required to store the kits, and the need to tear down and remake the kits should there be a short-term change in the schedule.

"All of these costs are a burden to the operation simply because accurate material inventories cannot be maintained and updated in ERP."

All of these costs are a burden to the operation simply because accurate material inventories cannot be maintained and updated in ERP. If they could be accurate, then the majority of the needless buffer stock could be removed, with materials being prepared only as needed for immediate use on the production lines. Here is the opportunity to again use our "smart data" from the factory machines and processes.

The smart, or "Lean," approach to material management is a simple concept. Collecting accurate material usage and consumption data from the machines and processes means that Lean material-management software can, with the help of the bill of materials and schedule data, calculate the rate at which materials are being used. They also can predict when new materials are needed, either as replenishment of existing reels in use or as part of a product changeover. Delivering materials on a Lean "just-in-time" basis reduces the amount of material WIP needlessly stored on the shop-floor by more than 95%.

Partially used materials have an automatically and accurately maintained count on a per carrier basis, and so they can be reliably returned directly to the warehouse for reallocation to other work orders. The material flow is qualified at the materials verification stage, as materials are loaded on to feeders and/or as feeders are loaded on to specific machine locations. This is normally a standard feature for the machine software using "smart feeders," where the unique material IDs can seamlessly integrate the machine-centric material-management environment into that of the whole factory.

At a factory level, all of the material logistics jobs can be aggregated over all processes. These would include the put-away of materials into the warehouse, the pick of materials from the warehouse for production (including such rules as "first-in, first-out"), the transfer of materials to the machines and process, the return of the materials from the machine into the warehouse, and an integrity check of warehouse locations when there is available time. Logic within the logistics "engine" can again look forward at the expected material needs, predicting busy times for logistics operations and bringing forward certain tasks to smooth out the task loading. The implementation of such a logistics management system has been shown to reduce the need for material operators by around 30%.

All of this has been made possible through the use of the data collected from all of the machines and processes in the factory. Where a single format for the data collection has been adopted, such as the use of the Open Manufacturing Language (OML), it is quite a simple process to integrate all possible points of material consumption, including manual stations, repair stations, and even material quality-inspection processes.

However, this kind of solution has various layers. For example, machine vendors offer local material carousels or storage towers that store materials close to the line, which is of value when production of specific products is confined to specific lines. Moving materials from one line or shop-floor–area carousel to another should be avoided if possible. A simple kanban extension to the overall factory materials logistics engine, however, can also set up dynamic kanban controls for the flow of materials between warehouses, including even from external supplier warehouses as required. For many operations, a single warehouse is sufficient for a whole site. In other cases, a hierarchical series of warehouses may be used, especially in EMS companies that have dedicated lines to specific customer products.

As we can see, the smart Lean materials solution is quite distinct from the old-school material management practice. Rather than "pushing" materials out in kits based on a factory schedule well in advance, the Lean "pull" system ensures that only materials that are needed are on the shop-floor and that every consumption of material is accounted for. The ERP and associated MRP operation can now run far more efficiently, which can then typically help reduce warehouse stocks by around 50% because of increased inventory accuracy. With all of the other benefits realized, such as the reduction of WIP materials on the shop-floor, the space saving, the logistics savings, the removal of the need of physical stock check, and also the eliminated internal material shortages, a rapid ROI is assured, which, in some cases, has been demonstrated in a matter of a few weeks. Once again, this is clearly not just "smart for smart's" sake. Here is a real, tangible benefit that is just as applicable to EMS manufacturers as OEMs, even where consigned materials are used. Few other examples can demonstrate where such a modest investment has such a significant impact on the operation.

This is just one more example of the advanced application of data that we are now able to collect using a factory-standard specification such as OML. In the first part of this series, we saw the justification of the use of an approach based only on asset utilization and productivity enhancement. Now, we can add the supply-chain benefits on top of that. Next time, we will look for even more. **SMT**

Michael Ford is senior marketing development manager with Mentor Graphics Corporation Valor division. To read past columns, or to contact the author, click here.

MilAero007 Highlights

EMS Firm Printed Circuits Adds AS9100C Certification

Printed Circuits Corp. has received certification to the AS9100 Rev C Quality Standard for its Lilburn, Georgia manufacturing facility and corporate headquarters.

Kitron Strengthens Cooperation with Aidon OY

Kitron has received orders for Aidon RF communication modules valued at more than NOK100 million. The orders will be fulfilled during the next three years and increases the current business scope with Aidon.

Zentech Manufacturing Acquires Interconnect Design Solutions

The addition of IDS and their experienced design engineering team adds significantly to Zentech's already comprehensive Engineering Services capabilities.

Libra Industries' CTO Completes MVP Upgrade / Training

Libra Industries CTO Scott Fillebrown recently completed upgrades and training on the MVP Supra E AOI system in its Mentor facility. The Supra E is a leading AOI solution for SMT manufacturers.

Sparton Showcases Future Naval Capability

Sparton, working closely with the Naval Undersea Warfare Center (NUWC) and industry partners, demonstrated the launch of an UAV from Sparton's Hammerhead system at the recent Annual Navy Technology Exercise hosted by NUWC in Newport, Rhode Island.

Benchmark Electronics Appoints Paul Tufano as President & CEO

Benchmark Electronics Inc. has named Paul J. Tufano as president and chief executive officer, replacing Gayla J. Delly who has resigned from her positions as president, CEO and as a member of the board of directors.

Saab Dynamics Extends Collaboration with NOTE

NOTE has been selected as strategic supplier for one of Saab's business areas, with a new agreement signed relating to prototype and serial production of PCBAs.

Digicom Electronics Incorporates Nitrogen in Soldering and Reflow Processes to Maximize Device Reliability

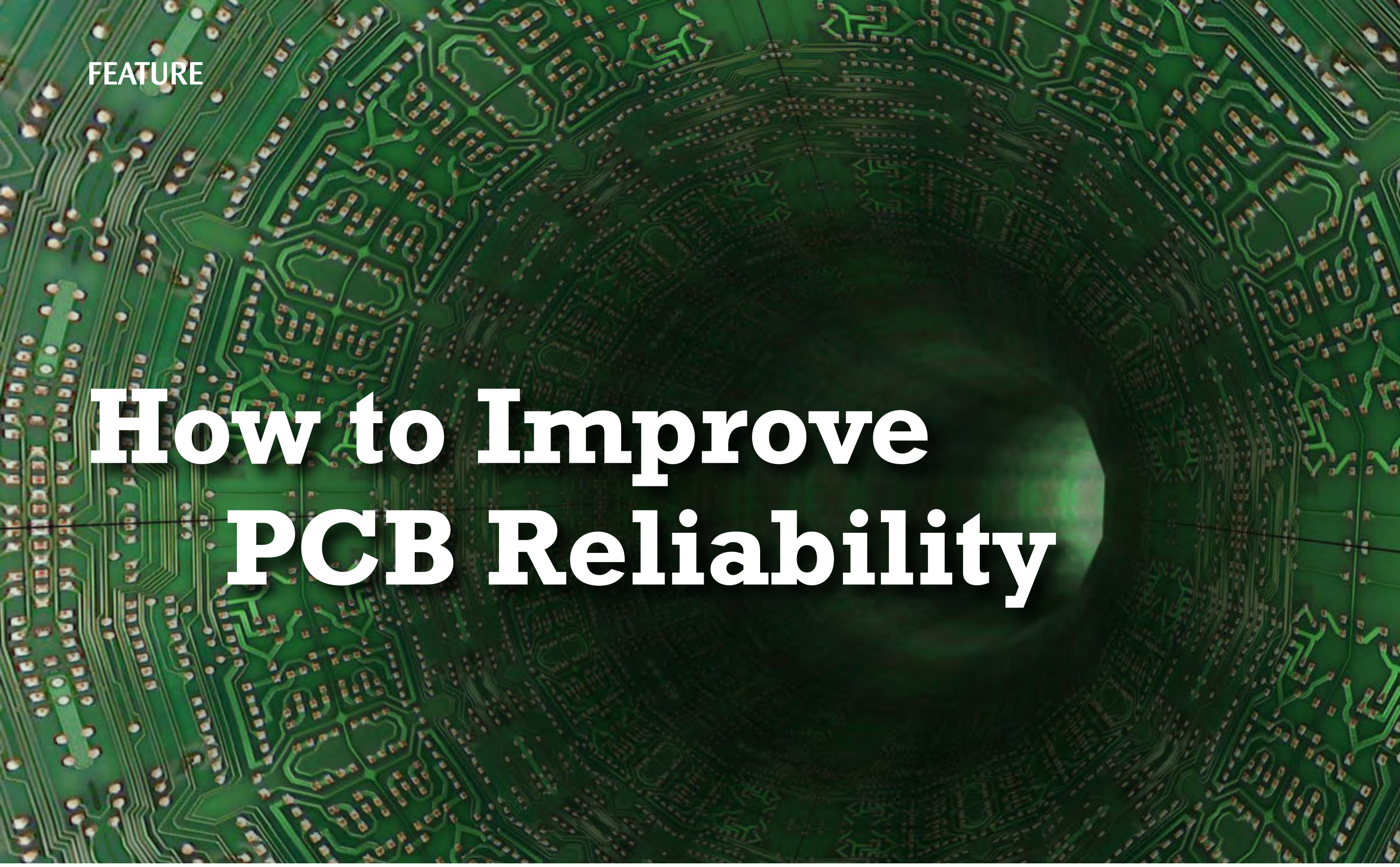
Digicom Electronics Inc. now generates its own nitrogen to use in its solder reflow, selective soldering, and hand soldering manufacturing processes to strengthen the bonds and improve solder adhesion.

Plexus Names Steve Frisch Chief Operating Officer

With his promotion to COO, Steve Frisch assumes responsibilities for Plexus' global manufacturing and engineering operations, go-to-market, supply chain, and quality functions.

Libra Industries Reports Growth Following the Acquisition of Texas EMS Provider

One year after its acquisition of ACD, Libra Industries has reported increased revenues and captured a greater share of the electronics contracting market.



How to Improve PCB Reliability

by Patrick McGoff
MENTOR GRAPHICS CORP.

If you research electronics reliability for the automotive industry, for example, you will find they all address only the electronic components mounted on a PCB. One of the more referenced reliability studies for the industry was conducted by Telcordia Technologies, titled, "Reliability, Prediction Procedure for Electronic Equipment (SR-332)." Like most other electronics reliability studies, it excludes the PCB.

Automotive manufacturers need to have stringent reliability requirements, and thus they have set goals for reducing component defect rates[1]. For example, a defect rate of less than 10 ppm for an engine control unit (ECU) or less than 1 ppm for a component within the ECU. The end game is "zero defect, zero failure."

The automotive industry has quantified the reliability rate for all the various component packages today and report defect rates as follows:

- ASIC—0.2 ppm
- Microprocessors—0.5 ppm
- Inductors—0.2 ppm
- Resistors—0.0 ppm

Component failure rates have steadily declined over the years to the point where non-component failure sources have become the dominant cause of failures for a PCB[2].

The problem with automotive-electronics reliability studies is they do not consider the PCB. If the reliability of the components is becoming a non-issue, then the only way to improve automotive electronics further is to look at the non-component aspects of the electronics, and a significant one is the PCB.

Each PCB design is a custom component, with its own unique, complex recipe:

- Material types and stackup
- Copper features
- Mechanical processes
- Chemical processes
- Electronic components
- Component mounting methodologies
- Impedance and capacitance concerns

All of the above form dependencies and constraints to every aspect of the PCB. How do you assess reliability for a "component" you have never used before? You measure the elements that make up the component, that is, the struc-

ture and features of the assembled PCB, including the solder-paste connection to the components.

First, measure and count the critical features of the PCB to assess the reliability of a custom component:

- Type of PCB—rigid, flex, flex-rigid, packaging substrate
- Size of PCB
- Number of layers
- Number of vias
- Size of vias
- Minimum annular ring
- Microvia stackup
- Number of component packages
- Double-sided SMT
- Range of package sizes
- Copper weight
- Copper distribution
- Test-point density
- Singulation method
- Zero-offset devices
- Gold fingers
- Vias in pad
- Embedded devices
- Aspect ratio

Second, list the electronic component and padstack details to be used to assess the reliability of a PCB assembly:

- Accurate body dimensions, preferably with tolerances
- Component standoff from PCB
- Lead type
- Pitch
- Smaller form packages are more susceptible to design and manufacturing issues
- Land pattern optimized for manufacturing
- TH pin diameter and length
- Solder mask-defined pads

Third, take into account the manufacturing processes used to produce the PCB:

- Conventional or sequential lamination
- Mechanical drill, laser drill or backdrill
- Number of panels stacked for drill
- Solder mask-defined pads
- Route or vscore singulation
- Flying prober or ICT
- Reflow, wave, or selective soldering
- Flow solder direction
- Conveyed edge for assembly
- SMT, auto-insertion, pressfit, or manual placement
- Stepped stencil
- Rework candidate

Manufacturing is a process, and processes also have tolerances. A reliability analysis needs

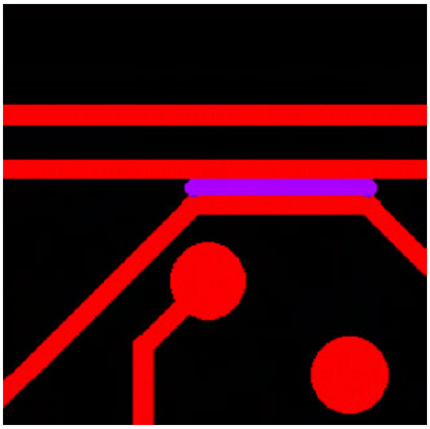


Figure 1: Close spacing over an extended length affects yield and reliability.

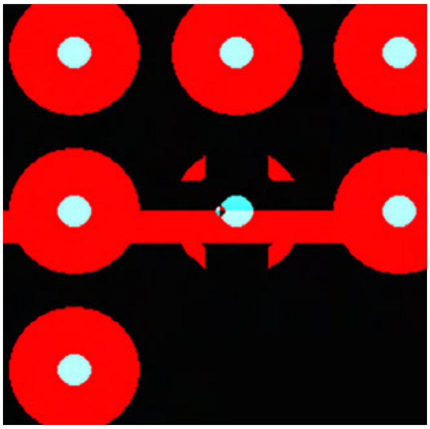


Figure 2: Starved thermals prevent proper heat containment, affecting the quality of via solder connections.

Figure 3: Manufacturing process tolerances can cause a same-net short, potentially affecting circuit behavior.

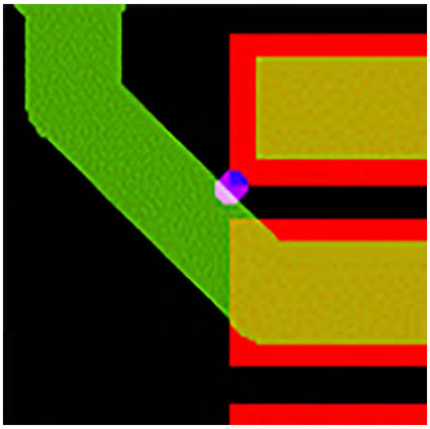


Figure 4: Circuits close to a pad must be fully covered by mask to avoid solder bridging during the assembly process.

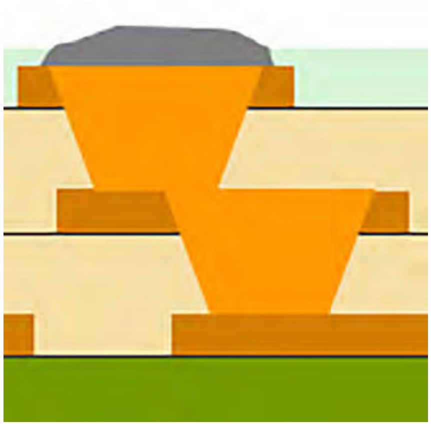


Figure 5: Via-to-via overlap in some cases is permissible and, in other cases, not.

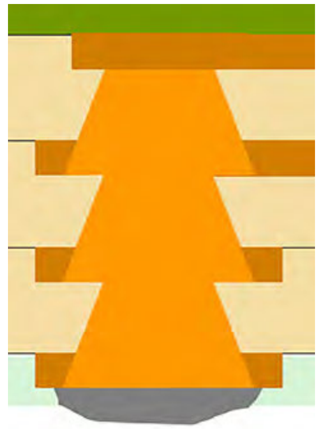


Figure 6: Stacked vias greater than three deep are at risk of collapsing without special processing.

to consider these fabrication tolerances. Figures 1–4 show some examples of issues found at fabrication that affect PCB reliability.

A 3-mil spacing for a length of 10 mil might be acceptable, but it increases the risk of shorts when it spans 100 mil.

This may result in the solder not wicking properly or evenly inside the hole, resulting in what could become a field failure.

Your CAD software permits this type of spacing for the same net; however, a short here could result in a critical net (controlled impedance, clock net, differential timing) that fails to perform as designed.

The challenge for many PCB designers is they do not see, at the design stage, the final solder mask openings the fabricator will use. These openings change in size and shape based on the fabricator's practice. Thus, potential bridging issues might not manifest until boards are built.

One of the more challenging areas to ensure quality in today's PCBs is with vias. Vias can take the form of plated-through holes mechanically drilled, microvias that are laser-formed, and backdrills that are mechanically drilled but are a secondary process and serve as an alternative to sequential lamination. Figures 5 and 6 illustrate a few rules to check for vias.

A different annular ring is often specified for the top, bottom, and inner pads on a microvia. Additionally, allowable annular ring varies according to drill size, board thickness, and plating type. Proximity to adjacent layer vias is also critical to measure.

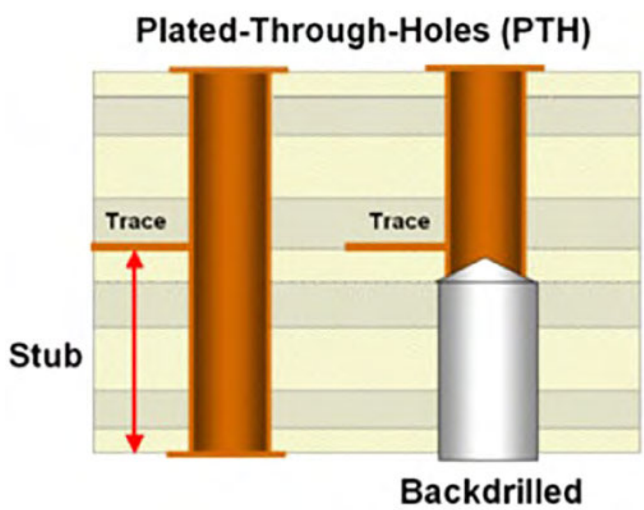


Figure 7: Check for backdrill depth tolerance so that the backdrill does not penetrate, or partially penetrate, the stop layer.

If you are using backdrill technology, make sure that you have a means to check for backdrill depth tolerance so that the backdrill does not penetrate, or partially penetrate, the stop layer (Figure 7). Also check for backdrill-spacing clearance to copper features throughout the stackup as you are introducing an additional

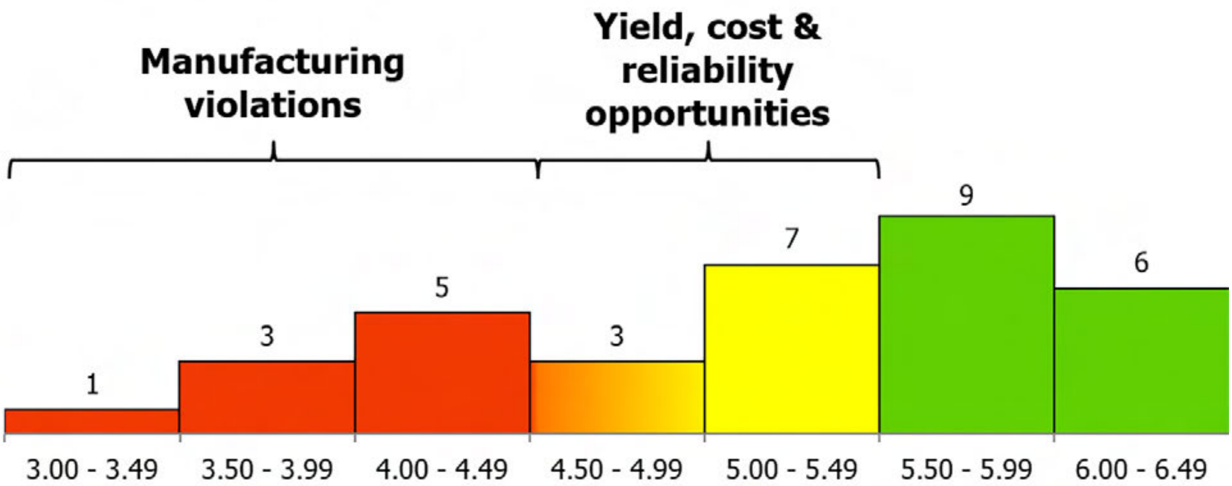


Figure 8: Using software to identify potential reliability issues with a design and that assigns a severity indicator to each instance is helpful.

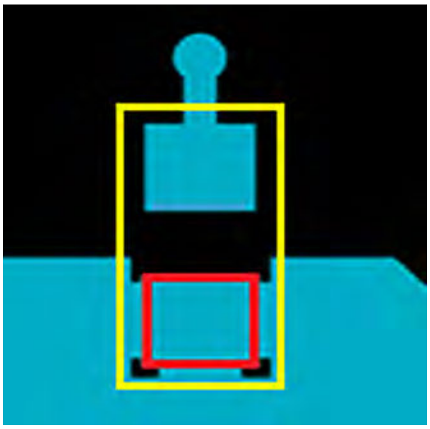


Figure 9: Connecting pads with different trace widths can cause the component to tombstone during reflow because of the variance in surface area.

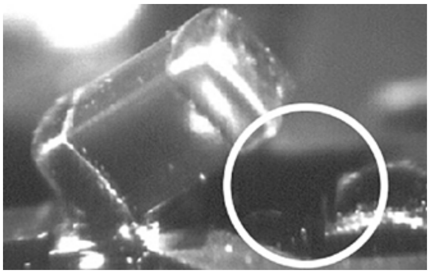


Figure 10: Resistor tombstoning caused by a difference in copper area on connecting pads.

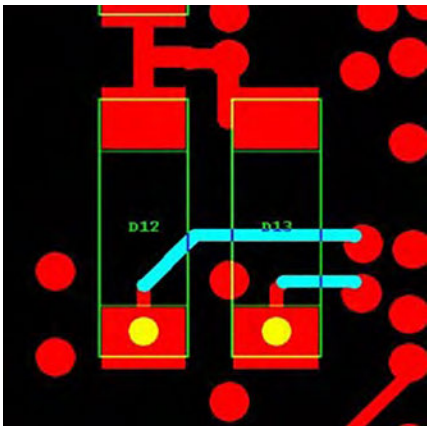


Figure 11: Traces under a no-lead device may cause the component to rock, or teeter-totter, because of the difference in height of solder mask and solder paste as the PCB goes through the reflow oven.

mechanical drill process. Clearly, you will need to maintain greater clearance to avoid creating a short or open in the backdrill process.

Many issues can prove to be problematic during the assembly and test stage as well. Most of the top 50 contract manufacturers worldwide perform some design-for-manufacturing (DFM) as a service. While this is valuable, each of them may approach the subject differently and thus you get a variety of responses. For example, some may show you where you can improve yield, cost, and reliability, while others may merely look to see that your design can be manufactured by them. One way to identify potential reliability issues with a design is to analyze it using software that will assign a severity indicator to each instance. After all, reliability is a probability of failure. Software tools that can pinpoint what issues are more likely to cause a failure can be quite helpful.

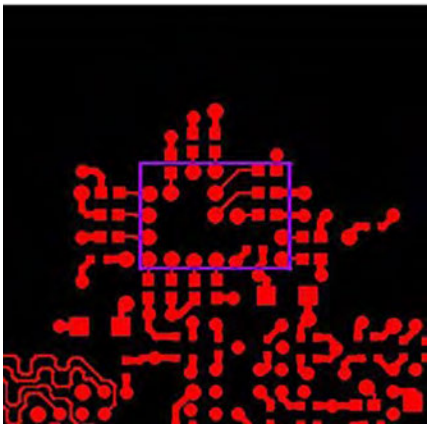


Figure 12: Too many ICT test points within an area will stress the solder joints in the area.

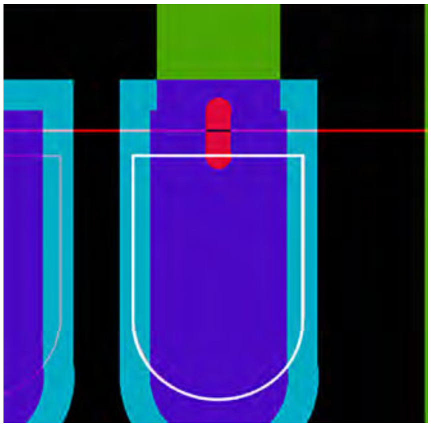


Figure 13: Insufficient heel distance and even the ratio of heel-to-toe distance can cause a weak solder joint. Conversely, too large of a pad for a device can cause a dry solder joint.

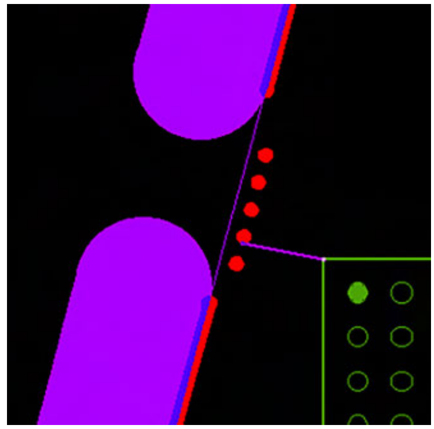
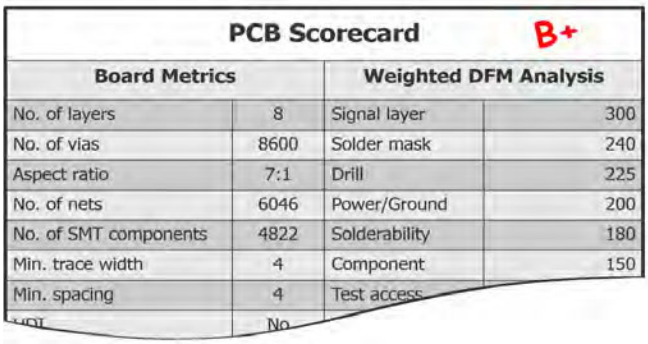


Figure 14: Placing breakaway tabs too close to SMD pads can result in damage to the solder joint when you separate the PCB from the panel.



PCB Scorecard B+			
Board Metrics		Weighted DFM Analysis	
No. of layers	8	Signal layer	300
No. of vias	8600	Solder mask	240
Aspect ratio	7:1	Drill	225
No. of nets	6046	Power/Ground	200
No. of SMT components	4822	Solderability	180
Min. trace width	4	Component	150
Min. spacing	4	Test access	
HDI	No		

Figure 15: The PCB scorecard will summarize your findings that can affect reliability.

Figures 9–14 show some examples of reliability issues that can be introduced during the assembly and test stage.

If you are lucky, this issue will fail at electrical test. However, if the stress just makes the solder joints weak, the problem might not show up until the product is in the field. In automotive applications, electronics must operate in wide range of conditions. Under stress, the weakest part of the design will surface.

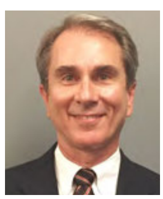
Once a PCB has been analyzed for issues that affect reliability, a scorecard can be made to summarize the findings. At this point, you'll want to assign appropriate weight to each factor because some issues are more critical or costly than others.

A PCB is constructed of thousands of elements, each of which can lead to failure in the field if not constructed in an optimal manner in relation to the other features. Remember, the reliability of the "custom" component is affected not just by the components on the top and bottom side of the PCB, but also the copper features throughout the PCB and the process means used to construct the PCB. If you can analyze the potential effect each of these elements has on reliability while you are in the design stage, you will improve the reliability of your end product. **SMT**

References

1. Bosch Design Requirements for Automotive Electronics, 2006.

2. A Practical MTBF Estimate for PCB Design Considering Component and Non-Component Failures, IEEE.



Patrick McGoff is a market development manager at Mentor Graphics Corp.

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Electronics Industry News
Market Highlights

NAND Flash Prices on Upswing in Q4 as Supply Shortage Becomes More Severe

The supply shortage that persisted in the NAND Flash market during the third quarter will become more acute in the fourth quarter due to surging demand from clients in the smartphone and SSD industries, according to industry analyst DRAMeXchange.

Four IC Industry Clusters Emerge with China's 13th Five-Year Plan

According to market research firm TrendForce, committed policy efforts and investments from the Chinese government have resulted in the formation of four IC industry clusters that are respectively located in the country's four major regions of activities – the Yangtze River Delta, the Pearl River Delta, the Beijing-Tianjin Bohai Sea region, and the Central-Western region.

Growing Demand for LEDs Vital for Global Market

Focusing on the development of energy-efficient LED lighting is likely to be a popular strategy among leading players in the global market in the coming years, according to a new report by Transparency Market Research.

IoT Revolution Revitalizes Demand for High-end Flexible Sensors

The global market for printed and flexible sensors is predicted to reach $7.51 billion by 2020, according to Transparency Market Research.

CIOs Must Design and Deploy Digital Business Technology Platform

Digital disruptors such as algorithms, AI, bots and chatbots are already transforming businesses. Gartner Inc. expects that algorithmic business will create even greater levels of disruption and new industries.

DRAM Module Industry Posted a 10% Decline in Annual Sales Revenue for 2015

The sales revenue of DRAM module worldwide for 2015 was around US$7.9 billion, representing a decrease of 10% compared with the 2014 figure, according to the latest revenue ranking of DRAM module makers by DRAMeXchange.

Medical Technology Device Market to Reach Nearly $240B in 2016

The market for medical technology devices is expected to reach nearly $240 billion in 2016 and this market is growing at a compound annual growth rate of 11% per year, according to a new study by Databeans Inc.

Note 7 Battery Fire Reveals Flaw in Samsung's Supply Chain Strategy

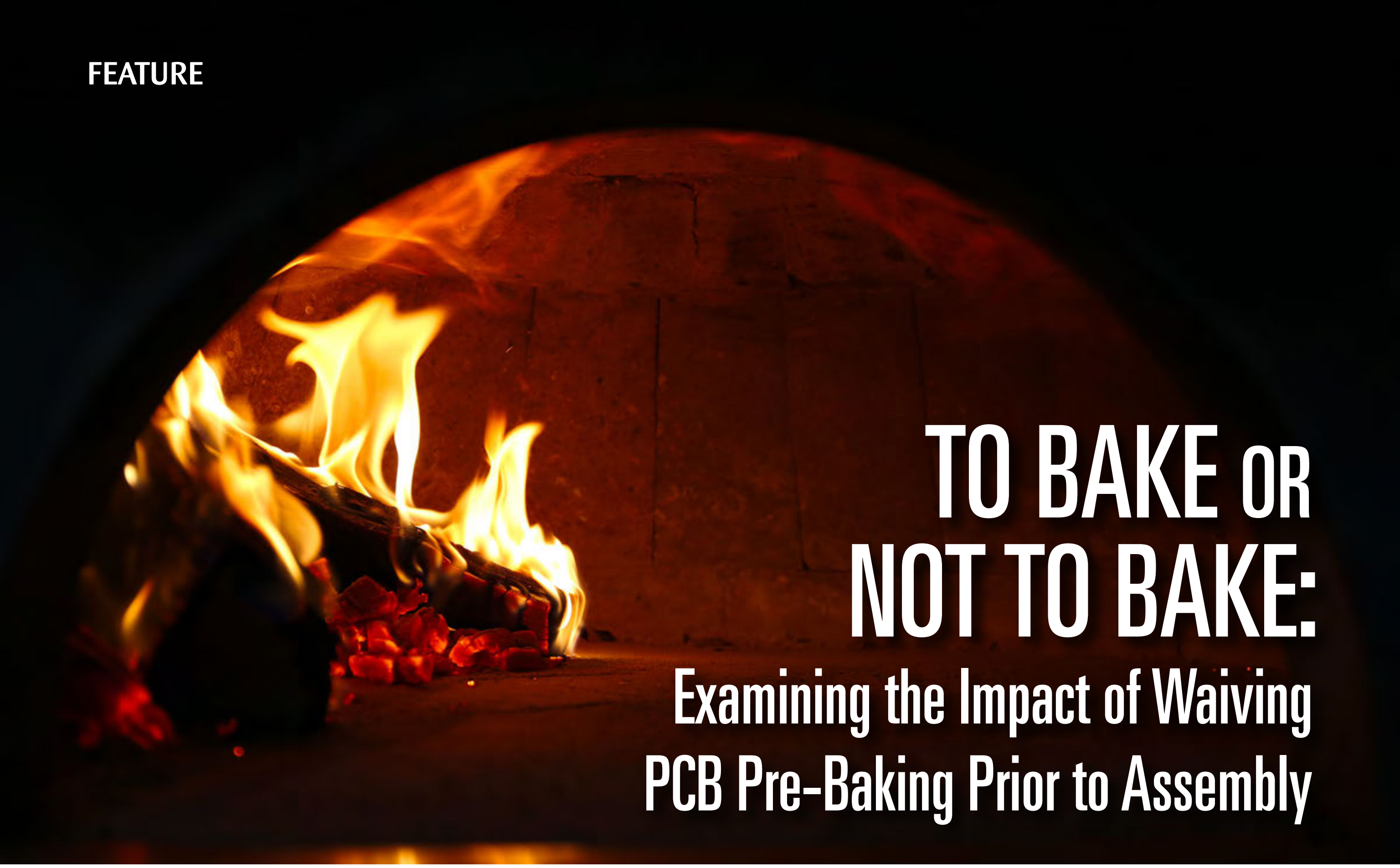
Battery fires linked to Samsung's latest flagship Galaxy Note 7 has led to a major fallout in the smartphone market, and is expected to cause smartphone brands to rethink their strategies for battery supply chains in the long run.

ADAS Market Poised for Growth

According to Transparency Market Research, the global advanced driver assistance systems market is expected to reach $50.48 billion by 2020.

APAC Maritime Defense Market Set to be Worth $185.8B in 2016

The Asia-Pacific maritime defense market is set to be worth $185.8 billion by the end of 2016 resulting from ongoing major naval expansion and modernization in China, India, Japan and South Korea and also though relatively major fleet upgrades in Indonesia, Malaysia, the Philippines and other national markets, according to visiongain.



TO BAKE OR NOT TO BAKE: Examining the Impact of Waiving PCB Pre-Baking Prior to Assembly

by Yash Sutariya
SATURN ELECTRONICS/SATURN FLEX

I'll always remember the summer of 2004 as the "Summer of Lead-Free." Finally, Pb-free circuit boards were going into standard production mode. Assemblers focused the majority of their efforts (often at my behest) on final finish and proper laminate selection. What none of us saw coming, however, was the rash of delamination that would burn the entire industry during that long, hot lead-free summer.

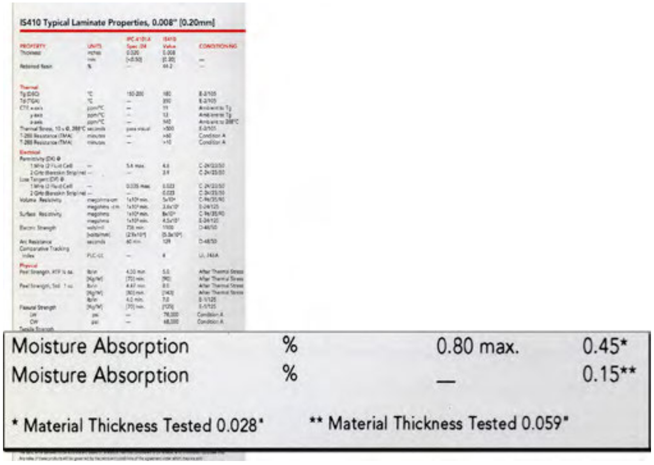
After a good amount of research, Isola came up with a Lead-Free PCB Fabrication and Assembly Guideline that outlined various steps in the PCB fabrication and assembly processes that are critical to successful lead-free PCB assemblies. The most prominent process step that was added in this guideline is baking—during fabrication and, most critically, just prior to assembly. The goal of baking is simply to drive moisture out of the PCB.

Moisture plays a critical role in lead-free PCB assembly. Therefore, it is important to discern the specifications of your base laminate. One knee-jerk reaction of North American PCB users was to specify what they believed to be the highest end laminates, those that qualify under IPC 4101/126 and /129 slash sheets. These are typically phenolic-cured materials, which have much higher thermal properties in terms of glass transition temperature (Tg) and decomposition temperature (Td) that are required to survive lead-free assembly without via failure.

Unfortunately, other properties of the laminate and assembly temperatures create a perfect storm for reliability failures. These include: moisture absorption, interlaminate adhesion strength, and water vapor pressure at lead-free assembly temperatures.

Moisture Absorption

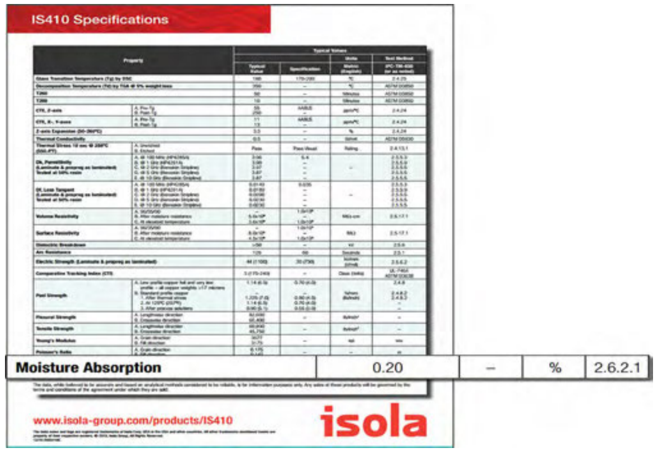
Moisture absorption of phenolic materials is more than 2x as compared to traditional FR-4 materials that qualify under IPC 4101/21. In the early days, the technical data sheets used a 0.028" thickness core material for moisture absorption measurement. Based on this test vehicle, phenolic laminates showed moisture absorption of 0.45%; comparatively standard FR-4 laminates scored a 0.20% rate of moisture absorption. Over time, I think someone got wise and changed the test vehicle to a 0.059" thickness core, thereby increasing the denominator



Moisture Absorption	%	0.80 max.	0.45*
Moisture Absorption	%	—	0.15**

* Material Thickness Tested 0.028" ** Material Thickness Tested 0.059"

Figure 1: Original phenolic laminate data sheet showing moisture absorption at 0.45%.



IS410 Specifications

Moisture Absorption	0.20	–	%	2.6.2.1

www.isola-group.com/products/IS410

isola

Figure 2: Current phenolic laminate data sheet showing moisture absorption at 0.20%.

Test Group - Standard FR4	Results
Peel Strength	
Condition:	Condition A:
Peel Strength Side 1	11.73 lbs / in
Peel Strength Side 2	10.95 lbs / in

Table 1.

Test Group - IPC 4101 / 129	Results
Peel Strength	
Condition:	Condition A:
Peel Strength Side 1	4.13 lbs / in
Peel Strength Side 2	3.85 lbs / in

Table 2.

of the weight loss calculation. This resulted in a moisture absorption rate of 0.20%, matching the rate of standard FR-4 laminate.

Copper Peel Strength (Used as a Measure of Interlaminate Adhesion)

Another critical characteristic affecting delamination is the interlaminate adhesion strength. In the past, we have tested standard FR-4 materials to be in the 10–12 lbs./inch range, as displayed in the Table 1..

Due to the difference in material composition, phenolic materials tend to have much lower peel strengths, typically in the 3–4 lb. range (Table 2).

The data suggests that the higher temperature, phenolic-cured lead-free capable laminates have only about one-third (1/3) the peel strength of standard FR-4 materials.

And Now... The Perfect Storm

Isola's studies suggest that vapor pressure of moisture in a PCB is 225psi at standard tin-lead (SnPb) reflow temperatures (approx. 200°C to 217°C). However, at lead-free reflow temperatures (approx. 250°C), the vapor pressure increases by about 2.5x to 550psi.

So, you now have a material that absorbs twice the moisture, has one-third the adhesion strength, and has to go up against 2.5x the vapor pressure. Nice.

This combination of factors is the primary reason we as fabricators have incorporated additional storage precautions and baking parameters in our processes. Unfortunately, the work doesn't stop here as there is responsibility upon the PCB user to pre-bake any re-absorbed moisture from the board just prior to assembly. Isola suggests baking per the following parameters (Table 3):

Final Finish	Temp	Time	Comments
Tin	125 °C	4 hours	Higher Temp may reduce solderability
Silver	150 °C	4 hours	Silver may tarnish but solderability not affected
ENIG	150 °C	4 hours	No issues with extended bake on ENIG finish
OSP	105 °C	2 hours	Long bakes may affect multiple heat cycle assembly

Table 3.

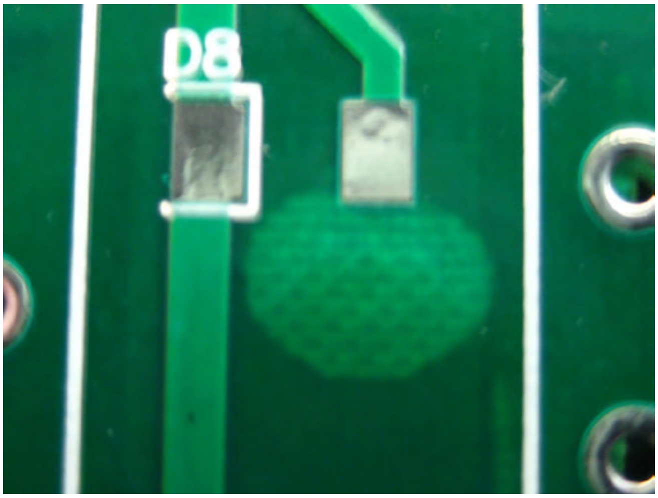


Figure 3: Example of surface delamination.

Figure 4: Example of board delamination.

Delamination Due to Moisture

Currently, pre-baking is avoided at many PCB assemblers due to the time and effort required for the process. Many of our customers consider the indicator of a successful lead-free PCB assembly process to be the lack of delamination. However, it is important to first look at what causes delamination.

As the moisture turns into water vapor, it exits the PCB. The most similar failure mode from the SnPb halcyon days are blowholes. Blowholes occur when moisture exits the PCB innerlayers through the copper plated hole walls—typically the weakest point on a PCB.

In lead-free PCBs, however, it appears that the laminate itself is the weakest point for vapor evacuation. In this case, the vapor seems to be exiting in a vertical (Z-axis), which is responsible for the ubiquitous cases of delamination.

That brings up a question, though. Just because a board hasn't delaminated, does that mean everything is OK? Or is there a negative impact on the vias from the mechanical stresses of water vapor escaping from the PCB?

Via Integrity

During the early days of the lead-free transition, I attended an Isola seminar focusing on laminate selection for Pb-free products. One of the salient points was that you can no longer rely solely on Tg for reliability. For example, their 170° Tg product, FR-4-06, only had a 290° Td vs. the 340° Td of their lead-free capable product. Life cycle testing revealed that vias had only 50% life (as measured by thermal cycling tests) as opposed to vias passed through a standard SnPb reflow process. Part of the reason for this was that the FR-4-06 had higher coefficient of thermal expansion (CTE) values than their new lead-free capable materials. What this tells me, though, is that the boards that were passed through lead-free assembly initially would have passed electrical and functional testing, and would then fail later on in the field (latent failure).

It seems like this portion of the seminar has been swept into the dustbin of history. Most folks today are only focusing on whether or not the PCB delaminates after assembly. If there is no delamination then the board is deemed reliable. But is that the whole truth?

Study for Via Life Impact

I designed an experiment testing this notion that an unbaked PCB that did not delaminate during initial testing is as reliable as a PCB that has been properly pre-baked prior to assembly. Here are the details:

Goal: The goal of this study is to determine the effect of properly pre-baking PCBs made from IPC 4101/126 or /129 laminate destined for lead-free reflow assembly.

Test Vehicle: For this study, we will use the Interconnect Stress Test (IST). This test uses specifically designed coupons that represent specific technologies. Electrical current is used to generate a thermal cycling environment that stresses the vias. Resistance is measured to determine via failure.

Our test panels represent a standard 8-layer PCB with 0.012" and 0.010" drilled hole sizes, representing a "heart of the range" of technologies.

Sample Preparation: We will pre-condition the test vehicles using three passes at a peak 245°C lead-free reflow profile.

Prior to this reflow pre-conditioning, however, we will add a moisture conditioning step as follows for three groups:

Group A: This sample set will be pre-conditioned by going through 8-hour live steam aging with five gallons of water. This will replicate one-year of shelf life under worst conditions.

Group B: This sample set will be pre-baked for four hours at 150°C, per Isola guidelines for lead-free laminates.

Group C: As is. These samples will be taken from a manufacturing environment, packaged, and dwell on a shelf for 30 days to replicate a standard dock-to-stock scenario.

IST Testing—Methodology [1]

The principles behind IST are actually quite simple. A current is passed through specific traces on a specially designed coupon. This current generates heat in those traces, which then heat the surrounding area to include vias, pads, laminate, etc. While the coupon is being thermal cycled in this manner, resistance is continually being monitored through the other traces and vias. Once the change in resistance measurement exceeds 10%, the coupon is deemed a failure and the number of cycles to that point are counted as passed cycles. Typically, the test is concluded after passing 500 cycles.

IST Testing—Results

Test 1: 8-hour steam + 3X Pb-free reflow:

TEST RESULTS

Coupon ID	Pwr Cycles	Pwr %	Sense Cycle	Sense %	Results
1a	1000	1.1	1000	1.2	Accept
1b	N/A	0.3	979	10	Sense
1c	1000	0.4	1000	1.4	Accept
1d	1000	0.8	1000	0.9	Accept
1e	1000	0.2	1000	0.3	Accept
1f	1000	1.1	1000	1.2	Accept
					Cus Spec
Mean	1000	0.6	996	2.5	N/A
Std Dev	0	0.4	9	3.7	
Min	1000	0.2	979	0.3	N/A
Max	1000	1.1	1000	10	
Range	0	0.9	21	9.7	
Coef Var	0%		0.86%		N/A

PRESCREEN RESULTS

Coupon ID	Power	Sense
1a	264.6	401
1b	260.6	416.6
1c	262.1	405.6
1d	254.8	379
1e	253.6	389.8
1f	253	365.3
Mean	258	393
Std Dev	5	19
Min	253	365
Max	265	417
Range	12	51
Coef Var	1.9%	4.8%

One coupon failed in the sense circuit (barrel) and all others passed to 1000 cycles.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Test 2: 4-hour bake @ 150°C + 3X Pb-free reflow:

TEST RESULTS

Coupon ID	Pwr Cycles	Pwr %	Sense Cycle	Sense %	Results
2a	1000	0.4	1000	0.7	Accept
2b	1000	-0.3	1000	-0.3	Accept
2c	1000	0.1	1000	0.2	Accept
2d	1000	0.2	1000	1.6	Accept
2e	1000	0.3	1000	0.4	Accept
2f	1000	0.3	1000	0.4	Accept
					Cus Spec
Mean	1000	0.2	1000	0.5	N/A
Std Dev	0	0.3	0	0.6	
Min	1000	-0.3	1000	-0.3	N/A
Max	1000	0.4	1000	1.6	
Range	0	0.7	0	1.8	
Coef Var	0%		0%		N/A

PRESCREEN RESULTS

Coupon ID	Power	Sense
2a	259.3	407.6
2b	259.8	393.6
2c	257.6	417
2d	253	404.8
2e	253	391.6
2f	252	377.1
Mean	256	399
Std Dev	4	14
Min	252	377
Max	260	417
Range	8	40
Coef Var	1.4%	3.5%

No failures to 1000 cycles.

Test 3: As is, 3X Pb-free reflow after receipt:

TEST RESULTS

Coupon ID	Pwr Cycles	Pwr %	Sense Cycle	Sense %	Results
3a	1000	0	1000	0.1	Accept
3b	1000	0.3	1000	0.6	Accept
3c	1000	0.1	1000	0.3	Accept
3d	1000	0.1	1000	0.2	Accept
3e	1000	0.3	1000	0.4	Accept
3f	1000	0.1	1000	0.2	Accept
					Cus Spec
Mean	1000	0.1	1000	0.3	N/A
Std Dev	0	0.1	0	0.2	
Min	1000	0	1000	0.1	N/A
Max	1000	0.3	1000	0.6	
Range	0	0.3	0	0.5	
Coef Var	0%		0%		N/A

PRESCREEN RESULTS

Coupon ID	Power	Sense
3a	264.6	409.8
3b	262.6	432.6
3c	262.6	421.3
3d	245	388.3
3e	248.5	403.1
3f	244.5	377.3
Mean	255	405
Std Dev	10	20
Min	244	377
Max	265	433
Range	20	55
Coef Var	3.8%	5.1%

No failures to 1000 cycles.

Conclusion

All coupons within all three test groups passed to 1,000 hours of IST testing. I was hoping to make a big splash but unfortunately the data doesn't support it. Effectively, boards built to IPC Class 3 specifications seemingly do not require pre-baking.

But what about boards built to Class 2 specifications? IPC Class 2 PCBs make up the vast majority of PCB designs. Our next step will be to duplicate this experiment using test vehicles plated to IPC Class 2 standards. If you are interested in receiving the results of this next test, please contact me. **SMT**

Reference

1. Further information on IST testing can be found here. I also found this nice write-up by Polar Instruments.

Yash Sutariya holds management positions at Saturn Electronics Corporation and Saturn Flex Systems Inc. To contact the author, click here.

Leadership in Your Company: Something to Worry About?

by Tom Borkes
THE JEFFERSON PROJECT

So, then, to every man his chance—to every man, regardless of his birth, his shining, golden opportunity—to every man the right to live, to work, to be himself, and to become whatever thing his manhood and his vision can combine to make him—this, seeker, is the promise of America.

—Thomas Wolfe, *You Can't Go Home Again*

This quote, dear reader, published in 1940, is the promise the founders had in mind when they constructed this country in the 18th century. They were leaders who believed that self-government (a new concept) was possible if the population was educated and virtuous.

It was clear that what Thomas Jefferson had in mind when writing the Declaration of Independence was not to create a new government that would guarantee equal results for all its citizens. Instead, he and the founders replaced the ruling English monarchy by constructing a government that created and maintained a free environment, one providing every individual with equal opportunity under the law.

However, the founders didn't just wave their arms and instantly produce a system that created the guaranteed opportunity they espoused. Instead, they produced a template for self-government based on principles that were invariant. The template is the Federal Constitution with an amendable Bill of Rights. The principles were those stated in the Declaration: life, liberty and the pursuit of happiness. As Martin Luther King Jr. said, the founders wrote a promissory note to those who at the time were not included as heirs to those natural principles. These were a set of lofty ideals for us as a country to run under over the years to come—two steps forward, one step back.

So the struggle continues to this day as the freedom and opportunity that Jefferson declared were inalienable individual rights are extended to more and more of the population.

The struggle has been most successful when the country's elected leaders have been true to the founder's objectives. However, our country's leaders have not been all elected. Martin Luther King Jr. was never elected to a government position, but few would deny that he was one of the greatest leaders the United States has ever produced.

This column will discuss the role of leadership in your company. Do you play a role in this rather amorphous subject? Leadership is an ingredient that most feel is important, even though many find it is hard to define. Some say that you will know good leadership when you see it.

Teaching Leadership

In some ways leadership skills mirror engineering skills in the difficulty academia has in making them relevant in the real world. Apart from getting really good at solving the odd-numbered problems at the end of the chapter, engineering academia preparing students for a career in high tech electronic product design and assembly has been and always will be ineffective in teaching the real-world skills industry needs. Certainly, we should expect no change if post-secondary education remains structured in the traditional way.

"Certainly, we should expect no change if post-secondary education remains structured in the traditional way."

As discussed in prior columns, important skills such as working in teams, solving problems without closed-form solutions, good judgment, conflict resolution and leadership, that are called upon frequently in the real world have little place on the college campus. Colleges and universities can teach the mechanics of using spreadsheets, budgeting, PERT charts, etc., but these are management, not leadership skills.

So, let's review:

In the September column[1], we concluded our six-part series with commentary on the current state of post-secondary education—one that leads to a career in the high tech electronic product assembly business. We demonstrated the acute need to significantly improve a student's academic preparation, both for the benefit of the student and the student's real world employer. This new teaching methodology called concurrent education should be applied to any dynamic engineering discipline or technology that changes more rapidly than academia has the ability to adapt to the change. In addition, the teaching strategy provides immediate value to the graduating student because it is a blend of learning for learning and learning for earning[1].

The Role of Leadership in Your Company

In the October issue, we launched a new series of columns focused on challenging our traditional organizational business structure. A structure that is hierarchical in nature and built upon the premise that it is best to collect employees of common skills into departments. Specifically, we challenged how our high tech electronic product assembly operations have been staffed and managed. In addition, we discussed the explicit and implicit roles leadership plays in a company's growth and prosperity[2].

We made the case that there is a huge difference between management and leadership. In fact, they are polar opposites! One of the reasons we have tended to lump them together is because they both involve planning, influencing and directing the activities of others in the organization.

Consequently, the costs associated with these activities are considered indirect and are burdened – i.e., they are estimated and absorbed in the direct labor sell rate. They are what contribute to raising a \$15.50 average hourly direct labor rate to, in some cases, a \$50.43 burdened hourly labor sell rate.[3]

What is the cost of management and leadership in your company? And, what does your company get for that money?

Over the next few columns we'll do a value assessment and try to quantify these indirect, overhead and G&A contributions and see if there are more cost effective alternatives available.

Shaping Your Company for Success

Whether you design, assemble, and sell your own products (as an OPD) or, provide manufacturing services for others (as an EMS provider) your company is evaluated by your customers in three general categories:

1. Price
2. Product or Service Quality
3. Performance (i.e., schedule compliance, reliability, feature desirability—if a product)

Unless you are a government employer, you perform on a landscape crowded with competitors. This landscape consists of rival companies that are all vying for similar business. What separates your company from the pack is how it is perceived in terms of the three metrics listed above. Price is clearly a heavily weighted criterion. However, price alone is not enough to imbue sufficient customer confidence to trust their franchise to an EMS provider, or result in sufficient sales to bestow the phrase "successful product" on an OPD.

It really comes down to the quality and competence of the people in the organization who are directly responsible for the design (if an OPD) and assembly of the product that greatly influence items 2 and 3, above—these are the direct employees.

Sixty years ago, the strategy to achieve product assembly quality was to inspect the quality into to product. In the limit the thought was if we could station an inspector behind every line operator we could assure product quality. There was even a department called Quality Assurance.

Even today some companies employ this strategy. Typically, those companies that cannot develop robust assembly processes are forced into inspection as the line of defense for their assembled product quality. As stated in an earlier column, in-circuit test (ICT) is a tool used in this product quality strategy. It adds no value to the customer. It merely is a consequence of a poor material supply chain, poor design, or an assembly process that is not statistically capable.

Employees help create the face of the company that employs them. Some companies like to showcase certain members of the workforce to their customers and conceal others. Why? Because some employees have better interpersonal skills than others. Those with good people skills and modest technical skills over time may gravitate to the sales and marketing departments.

"Most sales and marketing people are grown in the real world, not developed in the academic world."

Most sales and marketing people are grown in the real world, not developed in the academic world. At the risk of sounding like a broken record, academia is not an environment that can successfully act as a rehearsal hall for an engineer's performance in the real world—the learning for earning part. The same is true of sales and marketing people.

Leadership at the Top

If you had to name the one person who has the most influence in creating the face of your organization, who would that be?

I'm not Jewish, but have many Jewish friends. In fact, growing up on Long Island in New York (never say, in Long Island), going to elementary school I thought the world was primarily Jewish. I learned that there are two native languages: Hebrew and Yiddish. Yiddish developed as the language of the common people. It is a rich communicative source filled with idioms and expressive words and phrases, many of which have spilled into English parlance.

Here is the phrase that answers the question posed above:

די פיש סטינגקס פון די קאָפּ

Translated into English:
"The fish stinks from the head."

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So I would suggest that the person at the top in your company, the one with supreme authority, has the most influence in creating the face of your organization. Why? The company over time will take on the character and priorities of this person. If product and service quality really matter to her, the organization will begin to reflect this priority in hiring decisions. If quality is just window dressing, well, that will be reflected in the hiring policy, too. As employees who do not share these values leave the organization they will be back-filled with people who are more closely aligned with the top person's philosophy.

You and Your Company

I like to think about the unwritten employer/employee business relationship in a very stoic fashion:

1. The employee does the absolute best she can do for the company for a minimum of 40 hours per week (or, whatever is the standard salaried work week agreement).
2. The employee agrees to perform his job in accordance with company policy.
3. The employer (company) agrees to pay the employee an agreed upon salary in full and on time.
4. In addition, the employer will provide any benefits consistent with company's written benefit policy (e.g., medical, gain sharing, etc.).
5. Finally, the company will provide the employee with periodic performance reviews.

That's it!

Here's a question that is rarely asked; a question whose answer may seem obvious. Let's ask it anyway: Why do you work?

The answer that is probably the most common is, "I work to earn money to provide financial support for myself, or myself and my family."

However, there is another answer that is relevant to our discussion on leadership. "I work to be part of something larger than myself—and maybe something that can have a net positive impact on the human condition—something that I could not do alone."

I think this is true whether you work for a company or are self-employed.

We all have a dual nature. Call it what you will, but it is basically the internal struggle we all feel between right and wrong, between light and dark, between good and evil, between selfless and selfish. It is the reason movies like Lord of the Rings, The Chronicles of Narnia and Star Wars are so compelling: "Luke, come over to the dark side." And, in my opinion this is what leadership really is about—having the ability to persuade others to see the value in acting in the best interest of the project, the team, and the company.

A New Organizational Model

In many cases, the traditional hierarchal organizational model has had the opposite effect. In that model I am compelled to assign my personal allegiance to my department and to my department manager (the person who will evaluate my performance). Department "silos" are put in competition with each other. Finger pointing is a common practice.

As counterproductive as this model is, just as significant is the fact that it costs too much—it is burdened with indirect administrative cost that inflates the labor sell rate.

In upcoming columns, we will discuss details of a new model. This model is one that drastically flattens the organization. All departments are replaced with just two groups: product teams and a leadership group. There are three checks and balances on the self-managed product team's performance:

1. Other product team members
2. The leadership group
3. The applicable labor laws the company is subject to.

Since in the new organizational model, cross trained, multi-functional engineers will do everything including running the production lines, there will be no hourly workers. Everyone on the product team is a direct employee.

Most of the management for what can be termed the traditional general administration tasks will be done either by subcontractors or certain members of the leadership group. These

management tasks will be highly automated so the leadership group can focus on leadership.

An important role the leadership group will play is to effectively work for the product team. Again, this makes sense when you consider the leadership group is an indirect cost that must be absorbed in the direct labor sell rate. Besides being an important source of company leadership, their role includes acting as an enabling function. They are responsible for providing the product team with the tools and resources they need to be successful. This is in addition to their roles as a check and balance, resolving conflicts that the product team cannot solve themselves, setting a good example by always acting in accordance with company values and being responsible for looking beyond the horizon to ensure the job security of the product team members.

A Candid Assessment of Your Company's Leadership

And, that brings up an important point:

Look at the managers in your organization. Are they preoccupied with managing administration functions? If so, this distracts from their ability to be leaders.

What are the primary roles that the leaders in your organization should be playing? I would suggest that beyond persuading all employees to act in accordance with the best interest of the organization and promoting your company values through their example, it is providing for your job security and expanding opportunity for the advancement of the individuals in the workforce.

If some of those indirect personnel are not looking out over the horizon, challenging the company to minimize costs and ensuring that a reasonable order backlog is maintained. This results in your security and future are not being looked after.

It is sad when over the years I have encountered companies that have a downturn in business and conduct a layoff. This is a failure in leadership if it is backlog-related, and failure in management if it is cost-related. And, what normally happens is the direct labor force gets cut back—who, as I have said before, effectively, pays the salaries of indirect managers and leaders. Now, that is an injustice! It is company leadership and/or management that have failed—not the direct labor personnel who do their jobs day in and day out. It is members in the organization responsible for leadership and/or management who should be marched out the door, unless, of course, the manager and/or leader is a significant equity holder. If so, the board of directors needs to address the issue and remove the manager/leader part of this manager/owner's job description. Remember, "The fish stinks from the head."

Do you get the opportunity to review the performance of your managers and directors? If so, is the review anonymous? Does your company encourage constructive criticism? Do you get a chance to comment on the company's fidelity to the company mission statement and set of values (sometimes called a creed or "credo")? Does your company have a mission statement and credo? Does your manager assign responsibility without also providing the appropriate authority? Does your manager micro-manage—not properly delegating and not performing up to his job description?

"I have found many, if not most managers work down at least one job category. Directors do managers jobs, managers do group leader jobs, group leaders micromanage and do the work the engineers in their group should be doing."

I have found many, if not most managers work down at least one job category. Directors do managers jobs, managers do group leader jobs, group leaders micromanage and do the work the engineers in their group should be doing. This propensity for micromanagement is one that is common in engineering. Since no

one can do the job as well as you, and since you will be personally evaluated by the output of your group—just do it yourself. Believe me, from firsthand experience, learning to delegate is one of the most difficult skills for a young engineer to learn.

So the answer to the question, is leadership in your company something you should worry about, is yes, if the security of you job is something you care about and if the company growth that spawns individual opportunity and prosperity is important to you.

However, probably the most important thing is that company leaders don't have to be in management.

As we said last month, anyone in the organization can be a technical leader through demonstrating their mastery of the technical component of their job—but, more important they can be a leader of the workforce by putting their team, project and the company before themselves.

Finally, It's risky to be the little boy or girl on the parade route who screams, "The emperor has no clothes." However, this too is leadership. If your company cannot tolerate an assessment of this kind, maybe it's time to consider working for a different company.

Next month we'll continue to drill down into some of these topics and work toward a saner organizational structure—one that permits a more efficient and cost effective way to manage electronic product assembly and one that exploits the natural leadership abilities within the company.

Hey, what do you say? I'd like to hear your thoughts and experiences. **SMT**

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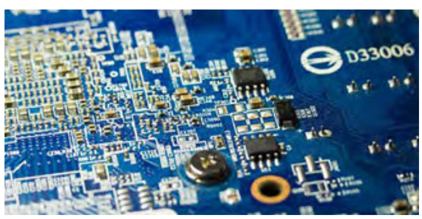
Tom Borkes is the founder of the Jefferson Project and the forthcoming Jefferson Institute of Technology. To reach Borkes, click here.

Engineers Design Ultralow Power Transistors That Could Function for Years Without a Battery



Engineers at the University of Cambridge have developed a new design for transistors that operate on scavenged energy from their environment. The design could form the basis for devices which function for months or years without a battery, and could be used for wearable or implantable electronics.

Using a similar principle to a computer in sleep mode, the new transistor harnesses a tiny leakage of electrical current, known as a near-off-state current, for its operations. This leak, like water dripping from a faulty tap, is a characteristic of all transistors, but this is the first time that it has been effectively captured and used functionally. The results, reported in the journal Science, open up new avenues for system design for the Internet of Things, in which most of the things we interact with every day are connected to the Internet.

The transistors can be produced at low temperatures and can be printed on almost any material, from glass and plastic to polyester and paper. They are based on a unique geometry which uses a 'non-desirable' characteristic, namely the point of contact between the metal and semiconducting components of a transistor, a so-called 'Schottky barrier'.

INCREASING RELIABILITY
Through Predictive Analysis

by Patty Goldman
I-CONNECT007

At SMTA International 2016, I caught up with Joe Russeau, president of Precision Analytical Laboratory, to discuss the paper he was presenting, which was co-authored by Mark Northrup and Tim Estes. Entitled, "Chemical Data vs. Electrical Data: Is One a Better Reliability Predictor," the paper presents early data comparing the results of two different analytical test methods to determine how well they correlate with each other as predictors of PC board cleanliness and reliability.

***Patty Goldman:** Joe, can you please tell me, and our readers, a little bit about your co-authors?*

Joe Russeau: Mark Northrup is the VP of Technology for IEC Electronics. He's the one that got us started on this project. Tim Estes is the CEO for Conductor Analysis Technologies.

***Goldman:** Tim is the PCQR² guy. So tell me about your involvement.*

Russeau: As for my involvement, I own and operate a cleanliness testing lab. My focus at the lab is on residue analysis, so we do ion chromatography, surface insulation resistance and electrochemical migration testing. In my view, the three of us, with our different backgrounds, were an excellent fit to work together on this kind of study.

***Goldman:** So tell us about the paper and what prompted this testing.*

Russeau: Basically our paper is trying to compare whether or not there's any correlation between the electrical data generated by the PCQR² test—that's a conductive anodic filament (CAF) test—and IPC's ion chromatography test (IPC-TM-650, method 2.3.28). The concern here is that within the industry, there is an increasing drive to smaller devices. Component population densities are increasing as board real estate shrinks. Hence, there is an increased urgency in understanding cleanliness impacts to product reliability and how to accurately measure those risks before product goes into the field. The ba-

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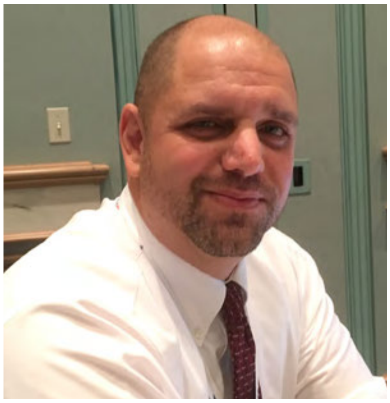
sis of the study was to compare what is currently available industry wide to ascertain which technique was better at predicting reliability. Mark Northrup, who is the primary researcher on this project, approached me and asked a couple of questions. The first question he asked was, "Do you know of any studies that show a correlation between the chromatography testing and any IPC electrical test?" To which I responded, "No, I wasn't aware of any." He followed up with a second question, which was, "Is one a better predictor of reliability?" To that I said, "I don't have an answer." Then he asked me if I'd be interested in participating in a study to try and determine an answer and that's how I got involved.


Joe Russeau

***Goldman:** I take it you guys have worked on this for some time now?*

Russeau: Well, Mark and I have had numerous discussions about the limitations of circuit board cleanliness testing for the past few years. Mark motivated us a little over a year ago to initiate this study, and we did the testing over a span of about six months. We looked at a total of eight different groups of CAF coupons. The CAF coupons we used were the ones that the PCQR² document calls out. We looked at the ionic cleanliness of the coupons before they went into CAF using ion chromatography as a baseline. Subsequently, these tested coupons were submitted for CAF testing. Upon completion of the CAF testing, coupons were retested via ion chromatography for cleanliness again. The idea was to compare residue levels before and after to determine what changes occurred and if the chromatography could predict a CAF failure. Our hypothesis was that we would see a correlation between the CAF and IC tests. We applied IEC Electronics ionic cleanliness limits to the ion chromatography test results and the current criteria used for the PCQR² test results to evaluate our hypothesis. We postulated that if there were residues that exceeded IEC Electronics ionic cleanliness limits before the CAF test, that corresponding failures should occur in the CAF test results. Of the eight groups, we had four groups that failed IC testing based on IEC Electronics ionic cleanliness limits and also failed CAF testing. The other four groups failed IEC Electronics ionic cleanliness limits, but passed CAF testing.

Based on this data, we drew the conclusion that there wasn't a significant correlation between the two tests, and in addition to that, we could not say definitively that either one of the tests was a better reliability predictor. We are still in the process of reviewing our methodologies and the variables that we want to do to try to improve the testing. We're just here today to present our initial data, hopefully get other people interested in the topic, solicit input as well for other ideas, and start a discussion of how to improve risk prediction for modern devices. Remember, this is just an initial test and is in no way definitive.

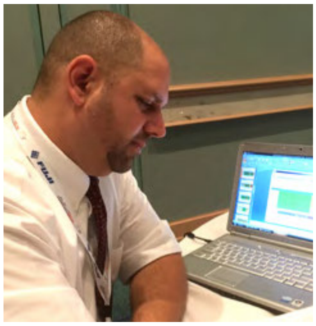
***Goldman:** I understand you're presenting some early data; it sounds like there's much more to be done.*

Russeau: That's correct. We have a lot more testing to do. Within IPC, I am the chairman of the 7-11 Test Methods subcommittee. I also sit on other task groups related to chromatography and board cleanliness. We deal with these issues within those task groups all the time. We know there are limitations in the IPC test methods and that industry demands improved testing methods as electronics continuously increase in density. We're working both from the standpoint of industry people who are coming together on their own to look for ways to make improvements, and then we're also supporting the IPC test methods committees (e.g., 7-11 subcommittee where we're starting to require validation of methods). Ultimately, we're trying to make sure that IPC test methods correlate and have solid data to support their intended purpose, so we can get to better reliability predictors.

***Goldman:* Yes. This interview should be an excellent way to perhaps encourage some other EMS providers to get involved in this.**

Russeau: Mark, Tim, and I would definitely like to see other people get involved—especially to help propose additional perspectives, provide parallel testing for correlation, and to continue to move the bar for IPC test methods capabilities higher.

***Goldman:* So you can expand it and get to some point where things either correlate, or come to some real conclusions here.**



Russeau: Yes, like I said earlier, with industry electronics companies designing tighter conductor spacing, smaller board real estate, and higher component densities there is a renewed interest in understanding what the cleanliness impacts are to those products and how to accurately predict those impacts before products go into service. Whether or not we find a correlation is anyone's guess at this point. There's not been enough data generated yet to remove uncertainty. Who knows, this ongoing testing may lead to an entirely new set of techniques to replace the current ones to support the electronics industry ever increasing demands.

***Goldman:* And also higher reliability is required, which is another side to that.**

Russeau: Absolutely. One of the other challenges that we have in reliability is differences involving environmentally friendly materials, both PCBs (e.g., halogen free) as well as fluxes (e.g., no-clean). Both are vastly different today than they were many years ago. The companies that manufacture these are trying to find better materials, with no negative impacts on reliability. Trying to match the methodologies we use for testing to keep up with those changes is becoming extraordinarily difficult.

***Goldman:* After this paper, what do you see as the next step?**

Russeau: Excellent question. We're still in the beginning stages of discussing that. What we're probably going to do is to see if we can home in on what the cleanliness requirements should be. As I mentioned earlier, the ion chromatography cleanliness levels that we used were IEC Electronics. They have a long history with using them. They have some level of confidence in those limits for harsh environments, but we have to decide whether or not they are applicable in how we're trying to use them for commercial, medical, industrial, and military environments in this testing. Remember, presently there are no ionic limits defined for either PBA or PB CAF testing. Add to this, another challenge since CAF is an inner layer board phenomena, so will IC testing predict it, or do we need to look at other types of test methods to be able to get in and see if there are other chemicals within the inner layers that are causing these problems? Like I said, this is just the beginning step to see if there is any correlation. There's much more work to be done.

***Goldman:* It seems like the importance of this isn't going to go away. It's only going to increase.**

Russeau: Correct, the importance of it is that we have to find ways of advancing the testing methodology to keep pace with the ever increasing electronics density technology. The ultimate goal is to improve our ability to risk mitigate and if we're using prehistoric methods from the '70s, '80s and '90s, then it is imperative that we update our testing methods and support them with strong data validation.

***Goldman:* Yes, that's a long time ago.**

Russeau: It is. So that's what Mark, Tim and I are trying to look at while asking for support from others going forward.

***Goldman:* Excellent. Joe, thank you so much for your time.**

Russeau: You're welcome. SMT

HKPCA's Daniel Chan on China's PCB Manufacturing and Technology Landscape

by Edy Yu
I-CONNECT007

Editor Edy Yu recently spoke with Daniel Chan, executive director of the Hong Kong Printed Circuit Association (HKPCA). Chan possesses more than 25 years of experience in global business management with strong leadership influencing suppliers and internal clients in business strategy and transformation. Prior to HKPCA, Chan had worked in IBM as the Global PCB Commodity Chairman, in the area of integrated supply chain management, quality assurance management, manufacturing and process engineering development and integrated product development. In this interview, Chan discusses the highlights of this year's International Printed Circuit and APEX South China Fair 2016, and he provides his insights on the current PCB technology and manufacturing landscape in China.

Edy Yu: What should we expect this year at the HKPCA & IPC Show?

Daniel Chan: The HKPCA & IPC Show is one of the most influential trade shows in the PCB and electronics assembly markets. It provides the industry with a premium platform for technology exchange as well as leading industry development.

This year's show theme is "Global Wisdom Shaping the Future," and is expected to attract close to 550 exhibitors from 17 countries and regions showcasing their latest innovations in more than 2,500 booths at Halls 1, 2 and 4 of the Shenzhen Convention and Exhibition Center. Our exhibition area now covers more than 50,000 square meters. Of the 550 exhibitors, 100 of them are new to the show.

We are also launching a new Japan/Korea Pavilion this year in Halls 1 and 2. This will group together the leading industry players from Japan and South Korea, bringing innovative equipment and technologies from these two countries to the show. As of September, it had attracted close to 30 exhibitors from Japan and South Korea, including JCU, Tsunoda, Taiyo Ink, Uyemura, Leadtech, Ishihara, NR G&C, MEC, Taesung, and GCE.

This year, the Smart Automation Pavilion will feature enriched content to help the industry progress towards higher productivity and more intelligent production. We are also bringing the Hand-Soldering Competition World Championship to the show, which will be its first time in China. Champions from China, Germany, the United States, South Korea and Japan will compete for the world title. Visitors will be able to observe the highest levels of hand-soldering craftsmanship at the event.

Other concurrent activities include the International Technical Conference, which will feature a variety of topics designed to bring you up to date on the latest technical and market trends in the industry. Meanwhile, the

Welcome Dinner and golf tournament will provide abundant opportunities to network with peers in a relaxed environment.

Yu: What can attendees expect at this show regarding current hot-button issues, such as the environment, smart manufacturing, and automotive electronics?

Chan: As a leading indicator of industry development, we follow market trends and stay on top of technology breakthroughs and innovations. Green development is still a sustainable topic in the industry and green production has increasingly become a typical configuration for PCB manufacturing. This year, the show's Green Pavilion will continue to provide the industry with a whole host of innovative green energy technology, new materials, and energy-saving production methods, to help enterprises carry out greener production.

To promote Industry 4.0 and Made in China 2025, and to strengthen our understanding of smart production, the Smart Automation Pavilion will be further enhanced this year to offer the latest automation equipment, technologies, and effective solutions that will help the industry move toward intelligent production and reduce labor cost.

The International Technical Conference will be held concurrently at the show, with industry experts sharing their insights on latest issues or solutions. Details will be announced soon.

Yu: Does PCB production technology development face any serious challenges today? What technology breakthroughs are you looking forward to seeing?

Chan: As the value-add of electronic products has increased, circuit board production technology is facing different challenges. From the HDI board point of view, as customer requirements and technology keep improving, manufacturers can now make 3+N+3 HDI boards, and 4+N+4 HDI boards are already on the way. After pressing the PCB more than three times, mostly because of alignment problems, the yield decreases. After multiple pressing, the movement between layers increases, posing a great challenge to the material. On top of this, circuit boards today are more sophisticated and signal transmissions are faster, requiring more accurate routing of boards. High-end boards now use semi-additive methods for production, which poses another challenge for HDI board production. As the circuit boards get smaller and more complicated, width and spacing will become even narrower, from the current 50 microns to 25 microns, and production yield of mobile phone PCBs will face a great challenge.

Daniel Chan

From the multilayer board point of view, high-frequency boards are facing signal integrity challenges. With the advent of 5G, routers and base stations' transmission speeds are expected to increase; in this case, material requirements and Df/Dk requirements are facing huge challenges. Circuit boards for supercomputers have as many as 40–50 layers. By using sequential lamination method, the alignment and drilling of the PCB and the connection of the inner hole of the HDI board are the technology bottlenecks in production. Material stability will also face challenges. In addition, as multilayer boards are getting thicker and thicker, and holes getting smaller and smaller, electroplating, filling, and high aspect ratio processes are also facing challenges.

In short, there are all kinds of different aspects of circuit board production technology bottlenecks, and it is difficult to determine which area will make a breakthrough first, but I think material stability, mechanical properties and plating technology need to be further improved.

***Yu:* What can you say about the current domestic PCB landscape, and your business development outlook in 2017?**

Chan: The domestic PCB industry is full of opportunities and challenges. China's electronics design community continues to grow, engaging in product design and the development of standards, such as mobile phones (Huawei), wireless base stations (Huawei, ZTE, Datang), and automotive parts. The development of the design segment is an opportunity. The challenges are coming from two drivers: The first is oversupply, which is causing great competitive pressure. In this case, prices go down and profits drop for domestic manufacturers. It could be a challenge, but it could also be an opportunity, because the cost of domestic manufacturing is relatively low.

Technical requirements are also challenging, because PCBs, especially electronic assembly and applications, get more and more complex. The required value-add and capabilities of PCBs are increasing. For example, mobile phone design is now more complex than ever; 5G technology is moving into the high-frequency domain; and routers and servers are getting even faster. Therefore, as domestic PCB production technology is relatively behind global technology levels, domestic PCB manufacturers need to catch up, narrow the gap, and work with other advanced countries with technology development, to have that innovative ability and meet the global market needs in the future. I am optimistic about the development of the domestic PCB industry, where there is still a huge demand for PCBs. When local manufacturers improve their technology, they will be able to expand their PCB business to the world, and solve technical problems that the domestic electronics industry is facing.

***Yu:* Many PCB manufacturers are now building their own PCB design team, while some are introducing SMT lines into the facility to expand their business. What do you think of this?**

Chan: This is the vertical integration of the whole industry, which goes from PCB production to SMT assembly and PCB design. Many of them are successful, such as Flextronics, Foxconn, Celestica and some other big enterprises. Companies that want to implement vertical integration need to gather their own technical capacity, as the technology in PCB industry is basically different from electronic assembly and electronic product design industries.

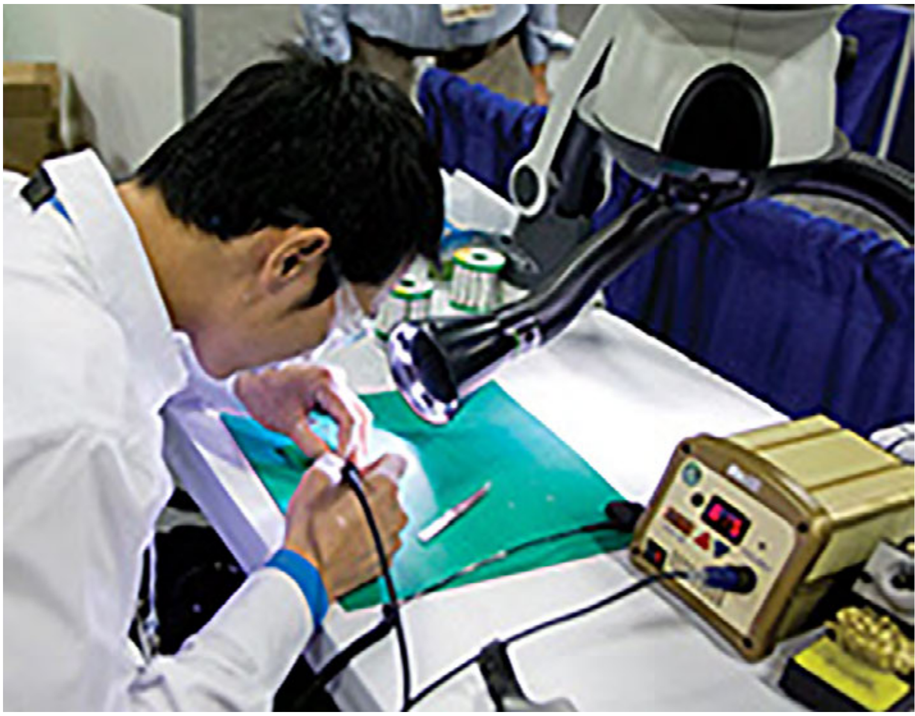
In general, PCB production is a mix of chemical, electronic, and physical engineering technology industries. Electronic product design basically belongs to the electronic engineering industry, which includes mechanical engineering, industrial engineering, automation engineering and a small amount of chemical engineering.

Overall, vertical integration is the right direction, which could control the whole chain better, but it is important that sufficient funds, personnel, and technical ability are provided to achieve the goal. Vertical integration also has its weak spot; it could lead to customer distrust, as customers would worry about their intellectual property leaking to the manufacturer's own design center or electronic assembly center. Therefore, PCB manufacturers need to establish independent operations that are separate from their associated PCB design company and electronic assembly company; otherwise, it will have an impact on their PCB sales. So manufacturers should separate the corporate image from the actual operation, which will have a positive effect on vertical integration development.

***Yu:* Thank you for your time.**

Chan: Thank you. **SMT**

HKPCA & IPC Bring Hand-Soldering Competition World Championships to China



by Edy Yu
I-CONNECT007

In an interview with Editor Edy Yu, Helen Guo, member services director at IPC Greater China, discusses IPC's activities and initiatives in China, such as standards development and promotion. She also discusses the upcoming International Printed Circuit and APEX South China Fair 2016, co-organized by HKPCA and IPC this year, which will feature the hand-soldering competition world championship for the first time in China.

Edy Yu: ***You have been hosting this show in China for many years. What's the purpose, and what has been achieved so far?***

Helen Guo: IPC's mission is to help our members achieve financial success and strengthen their competitive advantages. One of the ways we do this is by co-organizing this show to build a platform for industries to communicate, learn from each other, promote innovation, and facilitate cooperation.

After 15 years, the HKPCA & IPC Show has transcended its regional status and now attracts industry leaders and participants worldwide, becoming one of the most influential trade shows of its kind in the PCB and electronics assembly market. The event offers a premium platform for sourcing and technology exchange.

Yu: ***Smart manufacturing is on everyone's mind. How will they cover this topic?***

Guo: Industry 4.0 and Made in China 2025 are among the hottest issues in the industry. This year, the Smart Automation Pavilion will return with enriched content, bringing more innovative equipment, technologies and effective solutions that will help the industry move to more intelligent production and reduce labor cost.

Profit maximization and freeing labor forces for more creative work are driving industry changes right now. Intelligent manufacturing is going well in many industries, including the PCB and EMS sectors.

Helen Guo

Yu: ***Please tell us about IPC's specifications promotion and development in China.***

Guo: IPC specifications are evolving, with dozens of appropriate specifications being published each year. In technical, industrial and social development aspects, IPC is working very hard to develop new specifications, including revision updates. We have many of these specifications, such as the 1401 CSR (Corporate Social Responsibility) specification, and the 2581 series specifications (data transmission between automatic manufacturing and cooperation upstream and downstream). In addition, we are developing a press mounting specification in accordance with automotive requirements.

Yu: What's new at this year's hand-soldering competition?

Guo: The hand-soldering competition is one of our hit programs at the show, and it enables visitors to check out the outstanding soldering craftsmanship going on in the industry. This year, we are bringing the Hand Soldering Competition World Championship from the United States. It is the first time for this world championship to be staged in China, with champions from China, Germany, the United States, South Korea and Japan under one roof. We believe the three-day competition will see the highest levels of hand soldering craftsmanship anywhere.

Yu: Some PCB manufacturers are starting to develop their own PCB design capacity, while some are expanding their capabilities to SMT. What's your opinion on this?

Guo: It is normal for a company to expand or narrow their business scales as their advantages and resources change. We are happy to see that PCB makers are putting an effort into designing. Having the ability to design promotes a dynamic industry. IPC has abundant technology and intelligent resources to help companies enter an unfamiliar field and expand quickly.

Yu: Thank you for speaking with me today.

Guo: Thank you. **SMT**

ACHIEVING THE SMART FACTORY VISION

by Stephen Las Marias
I-CONNECT007

At the recent NEPCON South China event in Shenzhen, China, I was able to talk to James Liu, director of Standardization and Electronics Manufacturing at the Smart Factory Institute of the China Science and Technology Automation Alliance (CSAA), about how they can help small- and medium-sized companies in China transform their production into smart factories. He explained the challenges that these companies face, the future of automation in China, and the need for a free, open interface to connect disparate electronics manufacturing equipment and systems on the factory floor.

***Stephen Las Marias:** James, tell me about the Smart Factory Institute and your role in the company.*

James Liu: We use the Smart Factory name because we can give the industry the total solution for the smart factory. That's our mission, and that's my job, because I'm in charge of the electronics industry division. I was in IPC China for seven years, so I'm very familiar with the Chinese electronic industries. I want to develop a very useful solution for them, especially for the small- and medium-sized companies.

Our solution is quite different from the others. Many people know about smart factories. A very popular example is Siemens' Chengdu factory, a one-brand smart factory because all the equipment is made by Siemens. So it was easy to bring them together. In China, the situation is quite different. Almost every company uses various brands of equipment—different brands of screen printers, chip mounters, AOIs, and so on. It's difficult to link them into one system. However, in the electronic industry, automation right now is getting better. The concept of smart factories is automation plus cyber physical systems (CPS). That means we use the industrial Ethernet to link every piece of equipment. For Siemens, it's very easy because they manufactured all the equipment; but in China, it's very difficult because of the different equipment suppliers and the closed interface. Our solution is to develop a new interface that is free and open for the industry. That it my main job.

***Las Marias:** What would a smart factory look like for a small company here?*


James Liu

Liu: The smart factory means the production can be adjusted by the equipment itself. Also, it must be flexible. When you get an order, it gets sent to the designer and the designer gives them the specs. All the information is sent to the different equipment. The equipment runs automatically and the material control is also very flexible and automatic. For the electronics industry, the smart factory must be very flexible with a high level of automation.

Las Marias:* *You mentioned that you are focusing on the SMEs. Why is that?

Liu: In China, the very big companies are rich enough, so they contact big name companies. SMEs have lesser capital. They want to use their limited money to improve their production level. They need more help and they need more free counsel—and that's what we want to do.

Small and medium companies need to transform their operations into smart factories because the rules of the market have changed. Every user wants to use the equipment in their own way. They are always changing their requirements based on market demands. Manufacturers must follow these changes, so being flexible is very important. For a big company like Foxconn, which does mass production, there's no problem. But in the future, the market will have more and more need for people working on individual products. There will still be a need for mass production from the big companies, but smaller companies must focus on the low-volume production.

Las Marias:* *How will they justify their investments in transitioning to a smart factory?

Liu: They need to consult first. They have to know what they want to do and what their purpose is. Initially, they will tell us what their purpose is and what they want to do. Then we can help them with the design and maybe give some lectures or seminars to let them know what they need to do, step by step. Different companies have different requirements and different purposes, so we develop different solutions. We teach them because small and medium companies don't know what the smart factory should be; they just know they need to do this.

Right now, EMS companies are competing in price. Lower and lower prices cannot make money, so they want to get more orders, not only PCBAs, but they hope to get orders from the design through the final product. But they are not an OEM, so maybe this week they hope to get an order for a memory disc. Maybe next week, they will get an order for laptops. The change is huge and happens very frequently. Small- and medium-sized manufacturers face this situation. For mass production, Foxconn doesn't have that problem because they might only focus on one product, for example the iPhone, but smaller companies change between orders very frequently. A friend of mine has an EMS company and he told me every week they get 30 customer orders made up of 380 different kinds of products. In one week! They are always changing between products.

Las Marias:* *That's a big challenge.

Liu: Yes. So they have to use the smart factory to accommodate this.

***Las Marias:** Does your company only focus on China?*

Liu: Right now, we only focus on China because we know the situation and we can communicate with them very smoothly. Maybe in the future we can expand, but China is a very big market.

***Las Marias:** Earlier on you mentioned that you're planning to develop an open interface so that these different brand name machines will be able to communicate with each other. Can you explain how that works?*

Liu: The SMT line can work automatically because the interface is based off the SMEMA interface. It communicates to the screen printer and the pick-and-placer says, "I'm ready and please give me next the board." This communication is very easy, but the future smart factory needs to go to the pick-and-place directly without user intervention. The chip mounter and pick-and-place also report their situation so that you can collect the data and analyze if the machine is running well, or maybe yield is a bit down and needs to be fixed at once.

***Las Marias:** James, do you have any final words to say on the future of the smart factory?*

Liu: Maybe our interface is not the best interface, but I want to be a pioneer and launch this test before anyone else can do it. This is the key issue within the electronics industry—transitioning to the smart factory. And I want to overcome this problem. Maybe our interface is not as good, but maybe someone can develop better. That's good! I will continue to push this test forward, and it's my honor to do this.

***Las Marias:** James, thank you very much. I look forward to talking more with you about the progress of your endeavor.*

Liu: Thank you. **SMT**

Scientists Gain Insight on Mechanism of Unconventional Superconductivity

Researchers at the U.S. Department of Energy's Ames Laboratory and partner institutions conducted a systematic investigation into the properties of the newest family of unconventional superconducting materials, iron-based compounds. The study may help the scientific community discover new superconducting materials with unique properties.

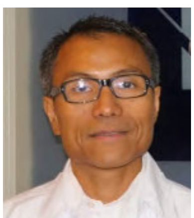
Researchers combined innovative crystal growth, highly sensitive magnetic measurements, and the controlled introduction of disorder through electron bombardment to create and study an entire range of compositions within a class of iron-based superconductors. They found that the key fundamental properties—transition temperature and magnetic field penetration depth — of these complex superconductors were dependent on composition and the degree of disorder in the material structure.

"This was a systematic approach to more fully understand the behavior of unconventional superconductors," said Ruslan Prozorov, Ames Laboratory faculty scientist and professor in the Department of Physics and Astronomy at Iowa State University. "We found that some proposed models of unconventional superconductivity in these iron-based compounds were compatible with our results, and this study further limited the possible theoretical mechanisms of superconductivity."

That information will also serve as a resource for future research into unconventional superconductors.

Recent Highlights from SMT007

1 Ionics EMS Talks Industry 4.0, Mil/Aero Opportunities, and Supply Chain



Dr. Jay Sabido, president and COO of Ionics EMS Inc., talks about a wide range of topics, including Industry 4.0, automation, and the challenges in the military and aerospace industry, including lead-free, counterfeit components, and traceability.

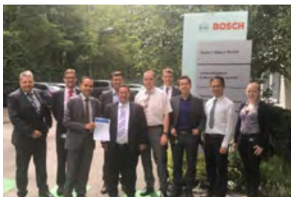
2 Rocket EMS Names Marla Sanchez CEO and Executive Director

Rocket EMS has appointed Marla Sanchez as CEO and Executive Director. She will succeed Craig Acuri, who is no longer with the company.

3 IPC to Debut Flexible Hybrid PEC Pavilion at IPC APEX EXPO 2017

IPC – Association Connecting Electronics Industries has announced that a new pavilion focusing on flexible hybrid printed electronics will debut at IPC APEX EXPO 2017 in San Diego.

4 LACROIX Electronics Named Preferred Supplier by Bosch Group



As a "Preferred Supplier" in the Bosch portfolio, LACROIX Electronics will be the first to be involved in the Bosch strategic and development projects, enhancing ability to plan ahead.

5 Celestica Awarded Excellence in Sustainability by Cisco

The award recognizes Celestica for demonstrating sustainability leadership above and beyond standard sustainability practices, and leading the industry through its approaches to reduce negative environmental impacts and raise positive social impacts.

6 Diffraction Taps OCM Manufacturing to Ramp Up Specialty Camera Production

OCM Manufacturing of Ottawa is providing design for manufacturing guidance in addition to turnkey manufacturing fulfillment for Diffraction's line of SBIC CCD cameras that serve the astronomy market.

7 IMI Mexico Achieves ISO 14001 Recertification

Integrated Micro-Electronics Inc.'s Mexico subsidiary, IMI Mexico, recently achieved ISO14001 recertification with no major or minor non conformity issue.

8 Electronic Systems Awarded 2016 Governor's Workplace Safety Award

Electronic Systems has received the Governor's Safety Award for Outstanding Achievement for its efforts in ensuring a safe work environment for all.

9 IPC Launches ESD Control Certification Courses on IPC EDGE

IPC has launched an ESD control certification course for electronics assembly trainers and operators through IPC EDGE.

10 Jabil Innovation Acceleration Services Help Customers Bring Products to Market Faster at Reduced Cost

Jabil Circuit Inc. is enhancing the value of its end-to-end manufacturing solutions through the introduction of new Innovation Acceleration Services that compress the entire product lifecycle—from gathering user insights and needs to shortening the path to commercialization.

SMT007.com for the latest SMT news and information—anywhere, anytime.

Events

For IPC's Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For the iNEMI Calendar, click here.

For a complete listing, check out SMT Magazine's full events calendar here.

IMPACT Europe 2016
November 1, 2016
Brussels, Belgium

PCB Carolina: Regional Trade Show
November 2, 2016
Raleigh, North Carolina, USA

electronica 2016
November 8–11, 2016
Munich, Germany

FUTURECAR: New Era of Automotive Electronics Workshop
November 9–10, 2016
Atlanta, Georgia, USA

Printed Electronics USA
November 16–17, 2016
Santa Clara, California, USA

ICT-UK Evening Seminar
December 1, 2016
Harrogate, North Yorkshire, UK

International Printed Circuit & Apex South China Fair (HKPCA)
December 7–9, 2016
Shenzhen, China

DesignCon 2017
January 31–February 2, 2017
Santa Clara, California, USA

MD&M West
February 7–9, 2017
Anaheim, California, USA

IPC APEX EXPO 2017
February 14–15, 2017
San Diego, California, USA

China International PCB & Assembly Show (CPCA)
March 2017
Shanghai, China

Thailand PCB Expo 2017
May 11–13, 2017
Bangkok, Thailand

JPCA Show 2017
June 7–9, 2017
Tokyo, Japan

PUBLISHER: **BARRY MATTIES**
barry@iconnect007.com

SALES MANAGER: **BARB HOCKADAY**
(916) 608-0660; barb@iconnect007.com

MARKETING SERVICES: **TOBEY MARSICOVETERE**
(916) 266-9160; tobey@iconnect007.com

EDITORIAL:
MANAGING EDITOR: **STEPHEN LAS MARIAS**
+63 906 479 5392; stephen@iconnect007.com

TECHNICAL EDITOR: **PETE STARKEY**
+44 (0) 1455 293333; pete@iconnect007.com

COVER: **SHELLY STEIN**

MAGAZINE PRODUCTION CREW:
PRODUCTION MANAGER: **SHELLY STEIN** shelly@iconnect007.com
MAGAZINE LAYOUT: **RON MEOGROSSI**
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